

CMOS Static RAM Memory Block for Embedded Design Applications (EmbSRAM)

Distinctive Features & Characteristics:

- Single widest Vcc operating voltages in industry, ranging from 2.4V to 5.5V.
- Fast Read access time, as fast as 35ns.
- Low power standby mode
- Provide high design flexibility for any number of read access bits (full custom design such as x8, x16 and xN per Read access).
- Small die size: 128Kb (450um x 450um ± 10% @ 0.5 technology).
- Also available and silicon proven in 0.35um technology.

Description

Aplus' 0.5um – 0.25um, 6T, 1P3M2W, 1024 bit SRAM memory block is a high-performance circuit block targeted for 100% compatibility with all of Aplus' non-volatile memories. The memory density varies from 8Kb to 4Mb to cover the full range of embedded SRAM applications. Access times are as fast as 35ns, and the circuit also offers a reduced power standby mode. When CEB goes HIGH, the circuit will automatically go to, and remain in, a standby power mode, as long as CEB remains HIGH. Significant system level power and cooling savings can be achieved by this capability. In addition, fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation.

Figure 1. Functional Block Diagram

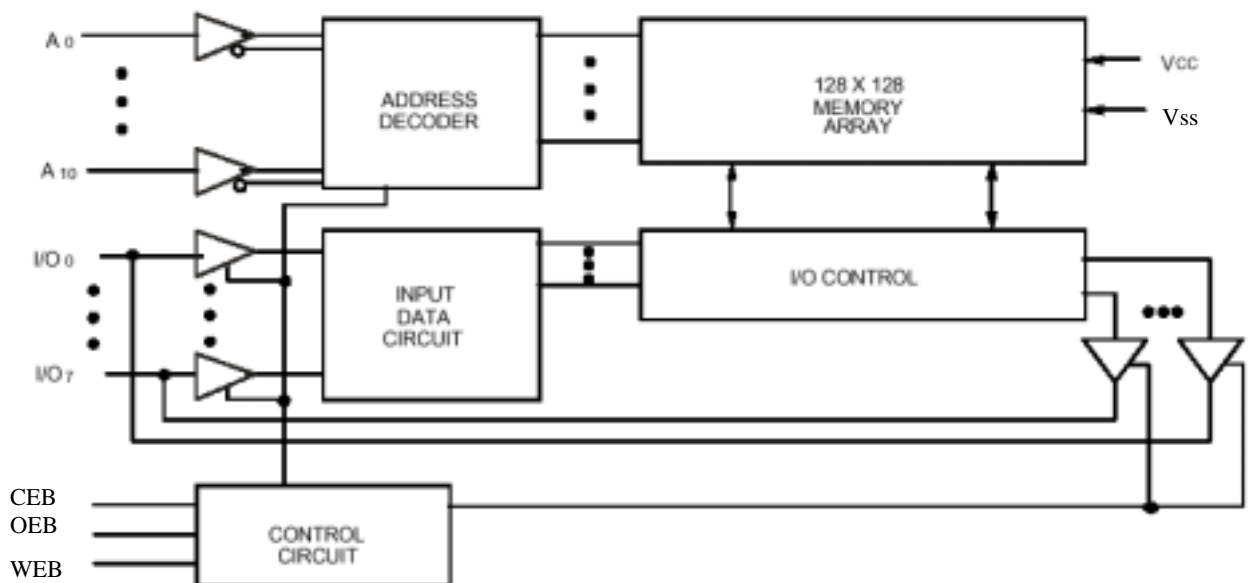


Table 1. Interface Signals Description:

Connector name	Type	Description
A0 – A6	Input	Address Inputs
I/O ₀ – I/O ₇	I/O	Data Input/Output
CEB	Input	Chip Enable
WE	Input	Write Enable
OE	Input	Output Enable
Vcc	Power	Low voltage power supply
Vss	Ground	Ground

Table 2: Capacitance (T_A = +25°C, f = 1.0MHz)

Parameter	Symbol	Min	Maximum	Unit
Address & Control Input Capacitance	C _{IN}	-	2	pF
I/O Capacitance	C _{I/O}	-	2	pF

Table 3: Truth Table

Mode	CEB	OEB	WE B	I/O
Standby	H	X	X	High-Z
Read	L	L	H	DATAout
Read	L	H	H	High-Z
Write	L	X	L	DATAin

Note:

1. H = V_{IH}, L = V_{IL}, X = Don't Care.

Table 4: Recommended Operating Temperature and Supply Voltage

Grade	Ambient Temperature	Vss	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

SRAM DC Characteristics

Table 5: Recommended DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V _{cc}	4.5	5.0	5.5	V
Ground	V _{ss}	0	0	0	V

Table 6: DC Electrical Characteristics

Parameter	Symbol	Typical	Maximum	Unit	Conditions
Read Current (Note 1,2)	I _{cc}	5	10	mA	@ 4MHz Read Cycle
Program Current	I _{pp}	20	40	mA	V _{PP} =12V, V _{cc} =6V
Standby Current	I _{SB}	10	100*	uA	*V _{cc} =max

Table 7: DC Electrical Characteristics

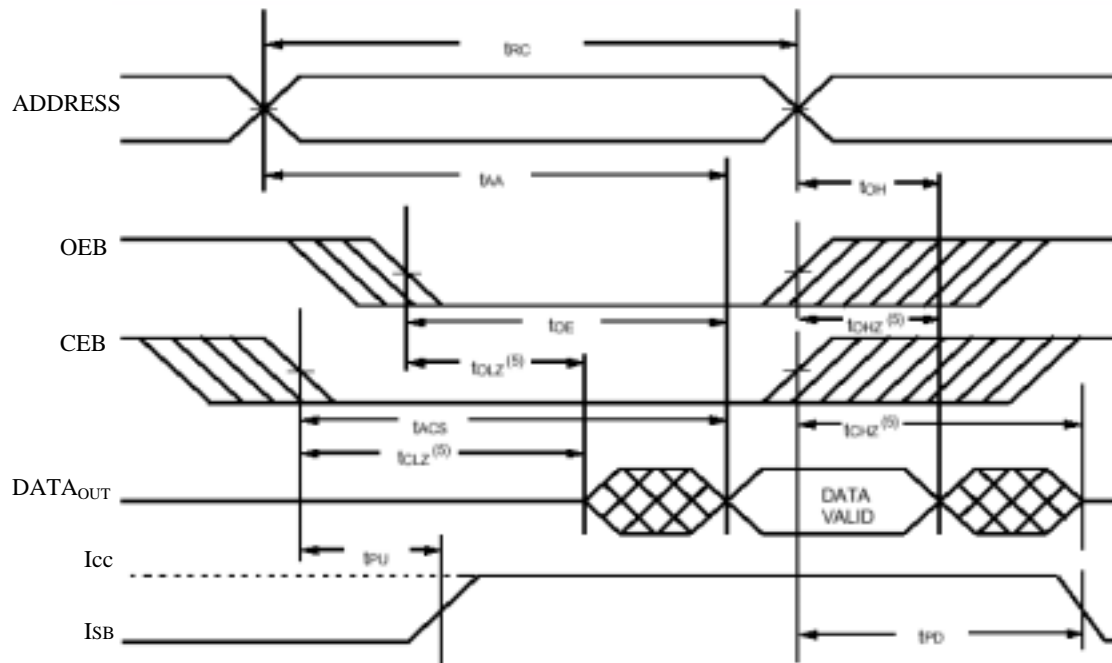
Parameter	Commercial & Industrial	Mil	Unit
Supply Voltage	V _{cc}	4.5	5.0
Ground	V _{ss}	0	0

SRAM AC Characteristics

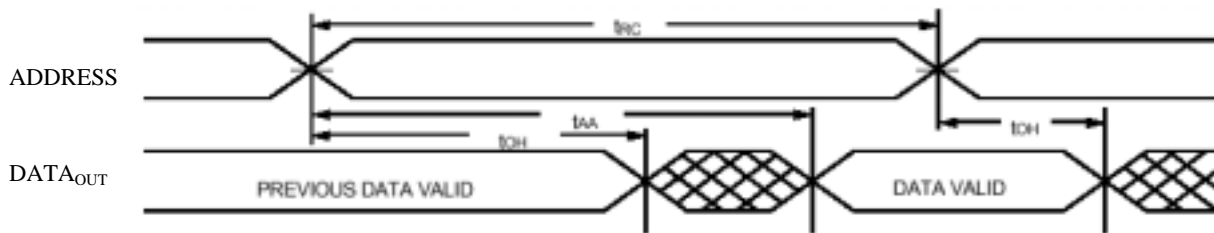
Table 8: Read Electrical Characteristics (V_{cc} = 5V ± 10%, All Temperature Ranges)

Parameter	Symbol	Min.	Max.	Unit
Read Cycle Time	t _{RC}	35	-	ns
Address Access Time	t _{AA}	-	35	ns
Chip Select Access Time	t _{ACS}	-	35	ns
Chip Select to Output in Low-Z	t _{CLZ}	5	-	ns
Output Enable to Output Valid	t _{OE}	-	20	ns
Output Enable to Output in Low-Z	t _{OLZ}	5	-	ns
Chip Deselect to Output in High-Z	t _{CHZ}	-	15	ns
Output Disable to Output in High-Z	t _{OHZ}	-	13	ns
Output Hold from Address Change	t _{OH}	5	-	ns
Chip Select to Power Up Time	t _{PU}	0	-	ns
Chip Deselect to Power Down Time	t _{PD}	-	35	ns

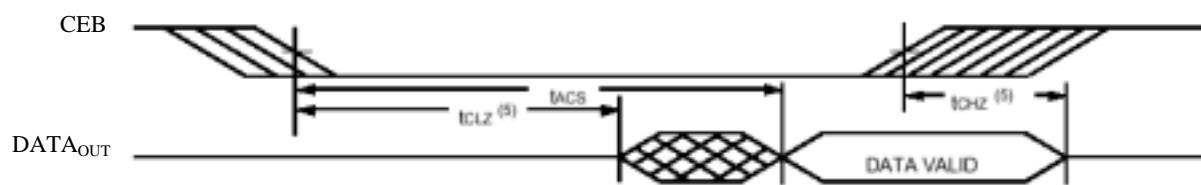
Timing Waveform of Read Cycle No.1^(1,3)



Timing Waveform of Read Cycle No.2^(1,2,4)



Timing Waveform of Read Cycle No.3^(1,3,4)



Notes:

1. WEB is HIGH for Read cycle.
2. Device is continuously selected, CEB is LOW.
3. Address valid prior to or coincident with CEB transition LOW.
4. OEB is LOW.
5. Transition is measured $\pm 500\text{mV}$ from steady state.

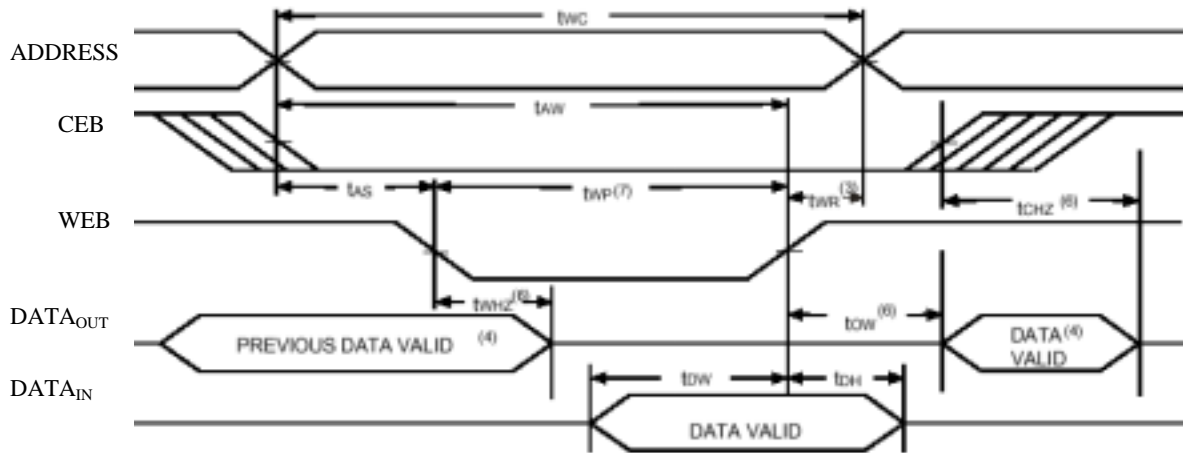
Table 8: Write Electrical Characteristics ($V_{CC} = 5V \pm 10\%$, All Temperature Ranges)

Parameter	Symbol	Min.	Max.	Unit
Write Cycle Time	t_{WC}	35	-	ns
Chip Select to End-of-Write	t_{CW}	25	-	ns
Address Valid to End-of-Write	t_{AW}	25	-	ns
Address Set-up Time	t_{AS}	0	-	ns
Write Pulse Width	t_{WP}	20	-	ns
Write Recovery Time	t_{WR}	0	-	ns
Write to Output in High-Z	t_{WHZ}	-	20	ns
Data to Write Time Overlap	t_{WC}	15	-	ns
Data Hold from Write Time	$t_{DH}^{(1)}$	0	-	ns
Output Active from End-of-Write	$t_{OW}^{(1)}$	0	-	ns

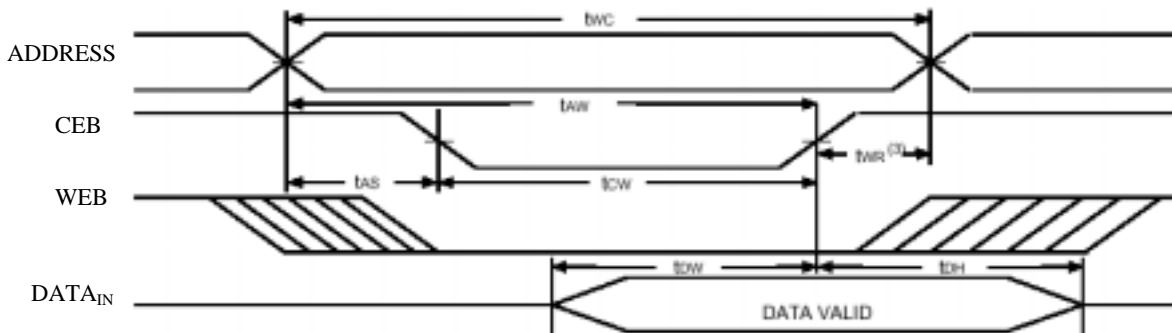
Notes:

1. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operation conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW} .

Timing Waveform of Write Cycle No.1 (WEB Controlled Timing) (1,2,5,7)



Timing Waveform of Write Cycle No. 2 (CEB Controlled Timing) (1,2,3,5,7)



Notes:

1. WEB or CEB must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW CED and LOW WEB.
3. t_{WR} is measured from the earlier of CEB or WEB going HIGH to the end of the write cycle
4. During this period, the I/O ins are in the output state and the input signals must not be applied.
5. If the CEB LOW transition occurs simultaneously with or after the WEB LOW transition, the outputs remain in the high-impedance state.
6. Transition is measured $\pm 500\text{mV}$ from steady state.
7. OEB is continuously HIGH. If OEB is LOW during a WEB controlled write cycle, the write pulse width must be the larger of t_{WP} or $(t_{WHZ} + t_{DW})$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW} . If OEB is HIGH during a WEB controlled write cycle, this requirement does not apply and the write pulse is the specified t_{WP} . For a CEB controlled write cycle, OEB may be LOW with no degradation to t_{CW} .

REVISIONS

Version Number	Description	Page	Date
0.1	First Preliminary Draft		4/07/03

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