OTP EPROM 2Mbit (256K x 8-bit)
AF27C020 (preliminary)

APLUS FLASH TECHNOLOGY, INC.
www.aplusflash.com

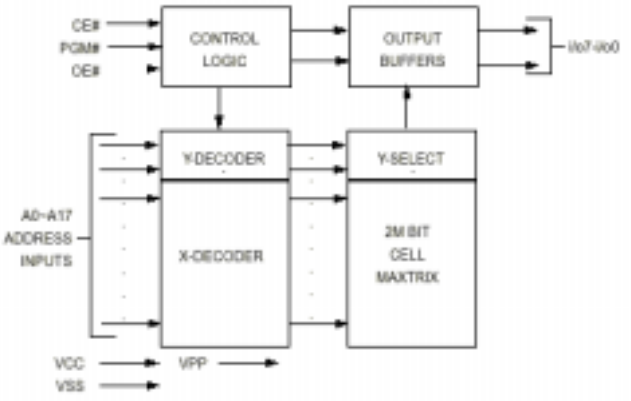
Features:

- 256K x 8 organization
- Single +5V VCC power supply ± 10% power supply tolerance standard
- Programming voltage of +12.75V ± 0.25V
- Fast access time: 70/90/120/150ns
- All inputs and outputs TTL compatible
- Current:
  - Operating: 30mA (max.) at 5MHz
  - Standby: 100µA (max.)
- Package type:
  - 32 pin plastic DIP
  - 32 pin SOP
  - 32 pin PLCC
  - 32 pin TSOP
- Compatible with JEDEC standard

General Description:

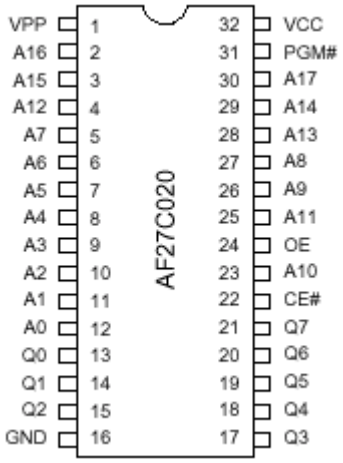
Aplus' AF27C020 is a high-performance 2Mbit One-Time-Programmable Read Only Memory. It is organized as 256K by 8 bits, operates from a single +5V VCC power supply and has all TTL compatible input and output signals. It also has static standby mode and features very fast single address location programming. For programming outside the system, existing EPROM programmers may be used, as it supports a fast programming algorithm time of less than one minute.

Block Diagram:



Pin Configuration

PDIP/SOP



TSOP

PLCC

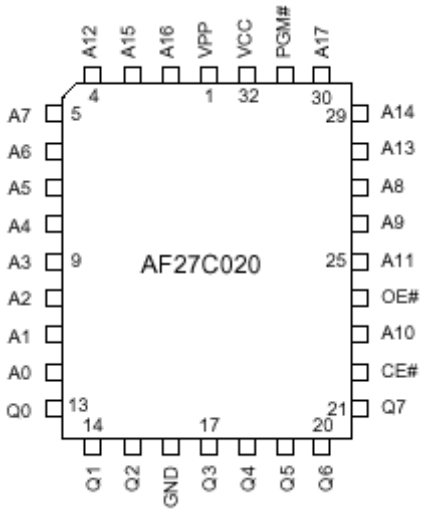


Table 1: Pin Configurations

Pin Name	Function
A0 – A17	Address Inputs
$I/O_7 – I/O_0$	Data inputs/Outputs
CE#	Chip Enable
OE#	Output Enable
PGM#	Program Strobe
VPP	Program Power Supply
VCC	Power Supply
GND	Ground

Table 2: Operating Modes and Truth Table

Mode	**CE#**	OE#	PGM#	A0	A1	A9	VPP	VCC	$I/O_7 – I/O_0$
Read	V_{IL}	V_{IL}	X	X	X	X	VCC	VCC	Data Out
Output Disable	V_{IL}	V_{IH}	X	X	X	X	VCC	VCC	Hi – Z
Standby	V_{IH}	X	X	X	X	X	VCC	VCC	Hi – Z
Program	V_{IL}	V_{IH}	V_{IL} PULSE	X	X	X	12.75V	6.25V	Data In
Program Verify	V_{IL}	V_{IL}	V_{IH}	X	X	X	12.75V	VCC	Data Out
Porgram Inhibit	V_{IH}	X	X	X	X	X	12.75V	6.25V	Hi – Z
Manufacturer Code	V_{IL}	V_{IL}	X	V_{IL}	V_{IH}	V_{ID}	VCC	VCC	26H
Device Code	V_{IL}	V_{IL}	X	V_{IH}	V_{IH}	V_{ID}	VCC	VCC	TBD
Continuation Code	V_{IL}	V_{IL}	X	V_{IL}	V_{IL}	V_{ID}	VCC	VCC	7FH
Continuation Code	V_{IL}	V_{IL}	X	V_{IH}	V_{IL}	V_{ID}	VCC	VCC	7FH

Notes:

1. X = Either V_{IH} or V_{IL}
2. V_{ID} = 12 ± 0.5V
3. A2 ~ A8 = A10 ~ A17 = V_{IL} (For auto identification)

Functional Description

Read Mode

The AF27C020 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable (CE#) is the power control and should be used for device selection. Output Enable (OE#) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (tACC) is equal to the delay from CE# to output (tCE). Data is available at the output after the falling edge of OE#, assuming that CE# has been LOW and addresses have been stable for at least tACC – tOE.

Standby Mode

The AF27C020 reduces the active current from 30mA to 100μA in its standby mode. It is placed in CMOS standby when CE# is at VCC± 0.3V. It also has a TTL-standby mode that reduces the maximum VCC current to 1mA. The AF27C020 is placed in standby mode by applying a CMOS high signal to CE#. When in standby mode, the output is in a high impedance state, independent of the OE# input.

Auto Identify Mode

The auto identify mode allows reading out of a binary code from an EPROM that will identify its manufacturer and device type. It is intended for programming equipment use by automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in ambient temperature ranges from 25°C ± 5°C.

To activate this mode, the programming equipment must apply voltages of 12V ± 0.5V on the address line A9 of the device. Two identification codes can be read from data output pin by toggling A0, when A1=V_{IH}. The other addresses must be held at V_{IL} during this mode. Byte 0 (A0 = V_{IL}, A1 = V_{IL}) & Byte 1 (A0= V_{IH}, A1=V_{IL}) represent the continuation code. Byte 2 (A0 = V_{IL}, A1 = V_{IH}) & Byte 3 (A0= V_{IH}, A1=V_{IH}) represent the manufacturer code and device code, which are 26H and TBD respectively. All identifiers for these codes will possess odd parity, with MSB (IO7) defined as the parity bit.

Absolute Maximum Ratings

RATING	VALUE
Ambient Operating Temperature	-40°C to 85°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to VCC +0.5V
VCC to Ground Potential	-0.5V to 7.0V
A9 & VPP	-0.5V to 13V

Notice: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this datasheet is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 3

Read Mode DC Electrical Characteristics (Ta = 0ºC to 70ºC, VCC = 5V ± 10%, VPP = VCC)

Symbol	Parameter	Min.	Max.	Unit	Conditions
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400µA
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.1mA
V_{IH}	Input High Voltage	2.0	VCC+0.5	V	
V_{IL}	Input Low Voltage	-0.3	0.8	V	
I_{LI}	Input Leakage Current	-10	+10	µA	VCC = max. V_{IN} = 0V to VCC
I_{LO}	Output Leakage Current	-10	+10	µA	VCC = max. Vout = 0V to VCC
I_{CC}	VCC Read Operating Current		30	mA	VCC = max. CE# = V_{IL}, OE# = V_{IH}, I_{OUT} = 0mA, at 5MHz
I_{SB}	VCC Standby Current (TTL)		1	mA	VCC = max. CE# = V_{IH}
I_{SB1}	VCC Standby Current (CMOS) (Note: In the min column 10µA is typical, not minimum. Isb1 specifications are at Vdd = 5.5V @ 85ºC.)	10	100	µA	VCC = max. CE# = VCC –0.2V
I_{PP}	VPP Current During Read		10	µA	CE# = OE# = V_{IL} VPP = VCC
I_{ID}	A9 Auto Select Current		100	µA	A9 = V_{ID} VCC = max.

Capacitance (Ta = 25ºC, f = 1.0MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_{IN}	Input Capacitance		6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance		12	pF	V_{OUT} = 0V

* These parameters are sampled and not 100% tested.

Table 4:

Read Mode AC Characteristics (Ta = 0ºC to 70ºC, VCC = 5V ± 10%, VPP = VCC)

Symbol	Parameter	70ns		90ns		120ns		150ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tCYC	Cycle Time	70		90		120		150		ns
tAA	Address Access Time		70		90		120		150	ns
tCE	Chip Enable Access Time		70		90		120		150	ns
tOE	Output Enable Access Time		40		45		50		65	ns
tOH	Output Hold after Address, CE# or OE#, whichever occurred first	0		0		0		0		ns
tHZ	Output High Z Delay		30		30		35		45	ns

Figure 1

Read Mode Switching Waveforms

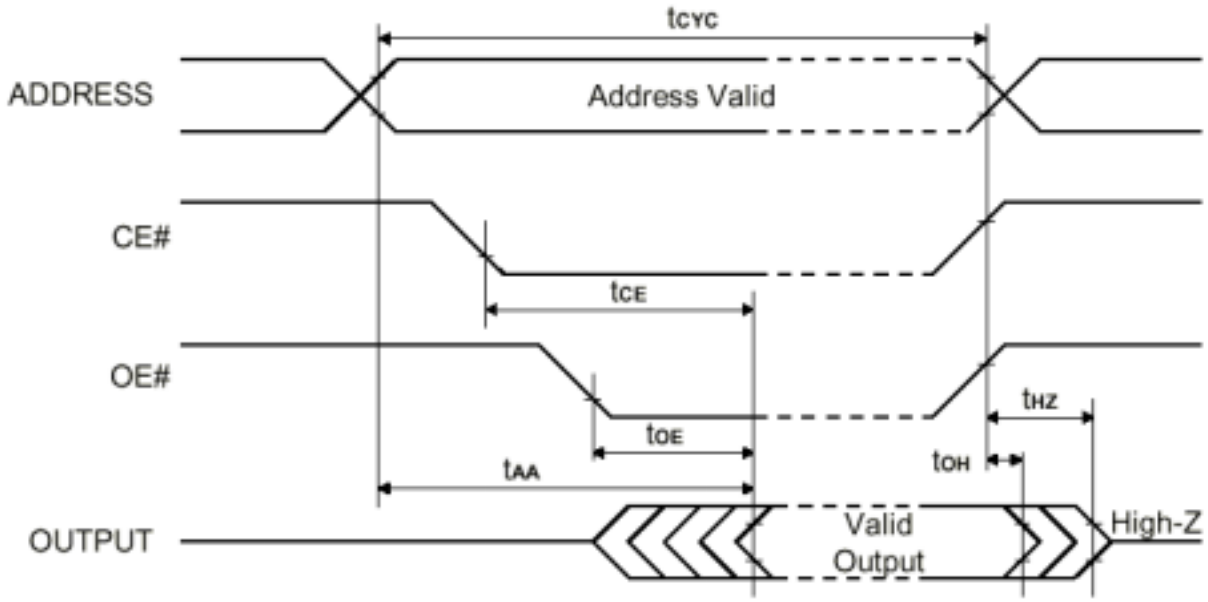


Figure 2

AC Measurement Conditions

for 70 ns ① Input Rise and Fall Times ≤ 10 ns
Input Pulse Voltage: 0.4V to 2.4Volt
Input and Output Timing Ref. Voltage: 0.8V to 2.0Volt

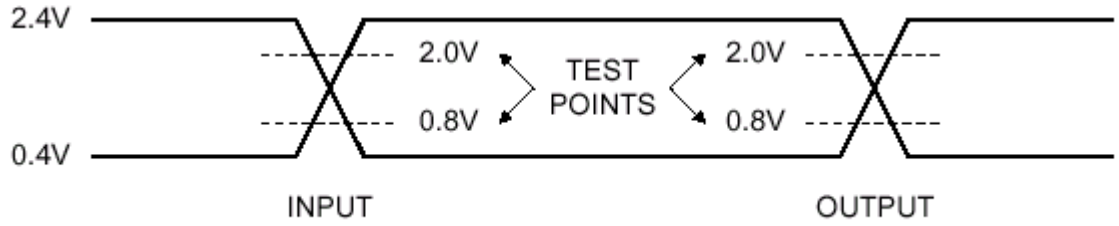
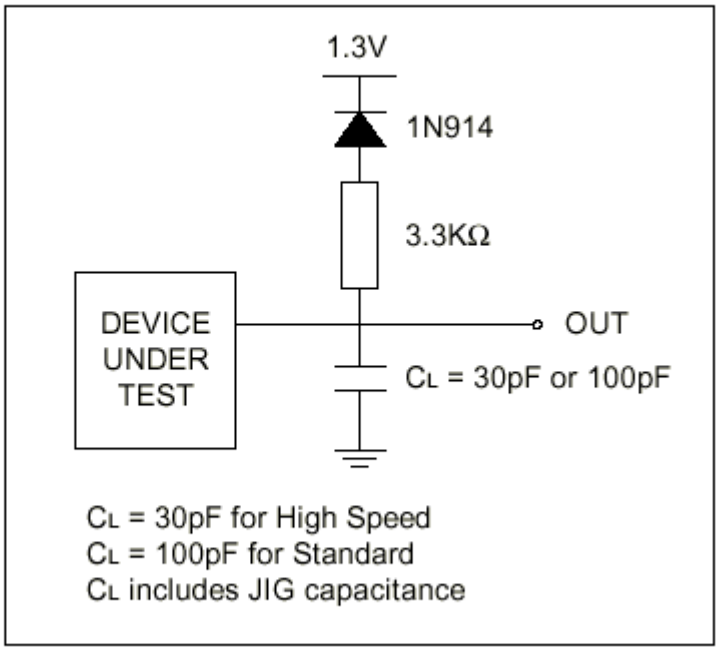


Figure 3

AC Testing Load Circuit



Programming and Program Verify

The AF27C020 is shipped with all bits in the '1' state. Data is introduced by selectively programming '0's into the desired bit locations. In the data word, both '1's and '0's will be present, although only '0's will be programmed. The programming mode is started when Vpp is at 12.75V, CE# and PGM# are at VIL, and OE# is at VIH. The data to be programmed is applied to 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

The write programming algorithm reduces programming time by using 100µs pulse followed by a byte verification to determine whether the byte has been successfully programmed. If the data does not pass the verification, an additional pulse programming is applied for a maximum of 25 pulses. The verified address is incremented. After the final address is completed, all bytes are verified again with VCC = 5.25V.

Program Inhibit

Programming of multiple AF27C020s in parallel is also possible with program inhibit mode. This mode is used to program OE#, PGM#, VPP, VCC, address bus and data bus, that are connected in parallel. When programming is performed, other AF27C020 can be inhibited from being programmed by setting their CE# pins to VIH.

Table 5

Programming Mode DC Characteristics (Ta = 0°C to 70°C, VCC = 6.25V ± 0.25V, VPP = 12.75V ± 0.25V)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400µA
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.1mA
V_{IH}	Input High Voltage	2.0	VCC + 0.5	V	
V_{IL}	Input Low Voltage	-0.5	0.8	V	
I_{LI}	Input Leakage Current	-10	+10	µA	VCC = max. Vin = 0V to VCC
I_{CC}	VCC Current During Program		50	mA	
I_{PP}	VPP Current During Program		50	mA	CE# = V_{IL}
V_{ID}	A9 Auto Select Voltage	11.5	12.5	V	A9 = V_{ID}
VCC1	Programming Supply Voltage	6.0	6.5	V	
VPP1	Programming Voltage	12.5	13	V	

Note: VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP.

Note:

1. VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP.

2. While programming, a 0.1uF capacitor is required across VPP and ground to suppress spurious voltage transients which may damage the device.

Table 6

Programming Mode AC Characteristics (Ta = 0°C to 70°C, VCC= 6.25V ± 0.25V, VPP = 12.75V ± 0.25V)

Symbol	Parameter	Min.	Max.	Unit
t_{AS}	Address Valid to Program Low	2		µs
t_{DS}	Input Valid to Program Low	2		µs
t_{VPS}	VPP High to Program Low	2		µs
t_{VCS}	VCC High to Program Low	2		µs
t_{CES}	CE# Low to Program Low	2		µs
t_{PW}	Program Pulse Width	95	105	µs
t_{DH}	Program High to Input transition	2		µs
t_{OES}	Input Transition to OE# Low	2		µs
t_{OE}	OE# Low to Output Valid		100	ns
t_{DHZ}	OE# High to Output Hi-Z		130	ns
t_{AH}	OE# High to Address Transition	0		ns

Figure 4

Programming and Verify Mode AC Waveforms

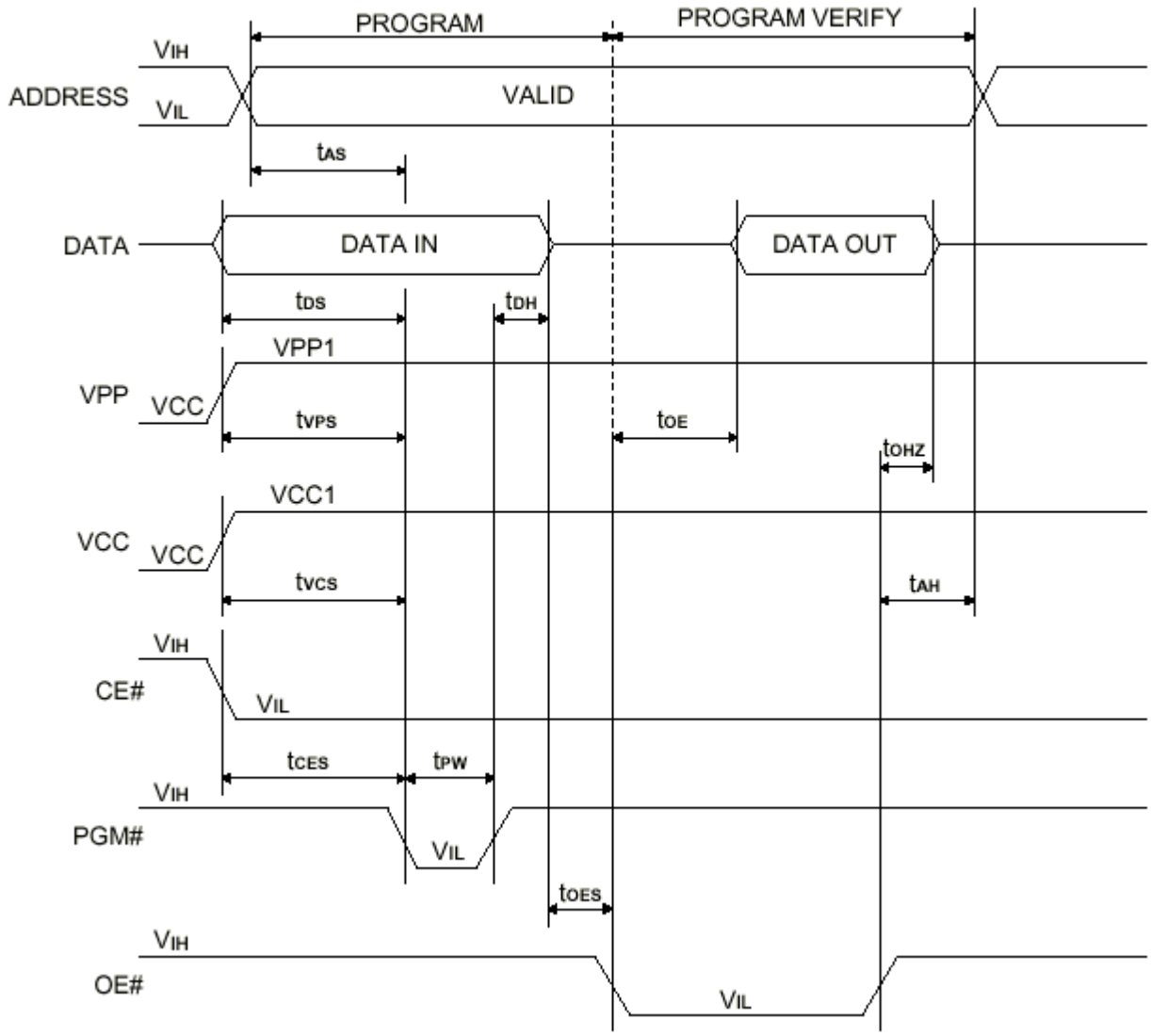


Figure 5

Programming Flowchart

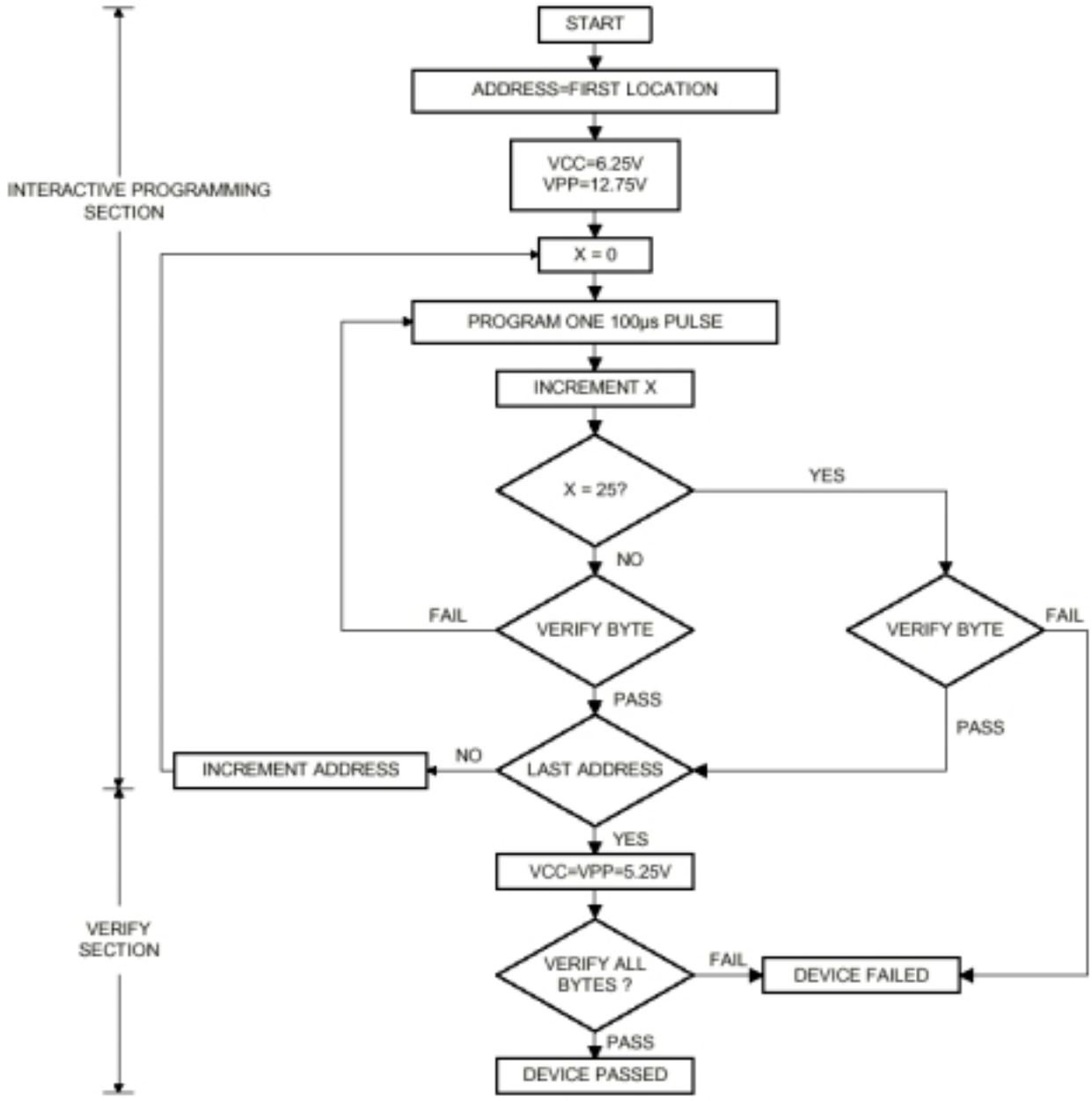


Table 7: PDIP32 – 32 lead Plastic DIP, 600 mils width, Package Dimensions

Symbol	Inch(Base)	MM(Ref.)
A	0.155 ± 0.008	3.937 ± 0.203
A1	0.025 ± 0.005	0.635 ± 0.127
B	0.018 (Ref.)	0.457 (Ref.)
B1	0.050 (Ref.)	1.270 (Ref.)
c	0.10 (Ref.)	0.254 (Ref.)
D	1.65 ± 0.005	41.91 ± 0.127
E	0.600 ± 0.005	15.240 ± 0.127
E1	0.550 ± 0.005	13.970 ± 0.127
e1	0.100 (Ref.)	2.540 (Ref.)
eA	0.650 ± 0.030	16.510 ± 0.762
L	0.13	3.30
Q1	0.0725 ± 0.005	1.8415 ± 0.127
S	0.075 ± 0.005	1.905 ± 0.127

Figure 6: PDIP32 – 32 lead Plastic DIP, 600 mils width, Package Outline

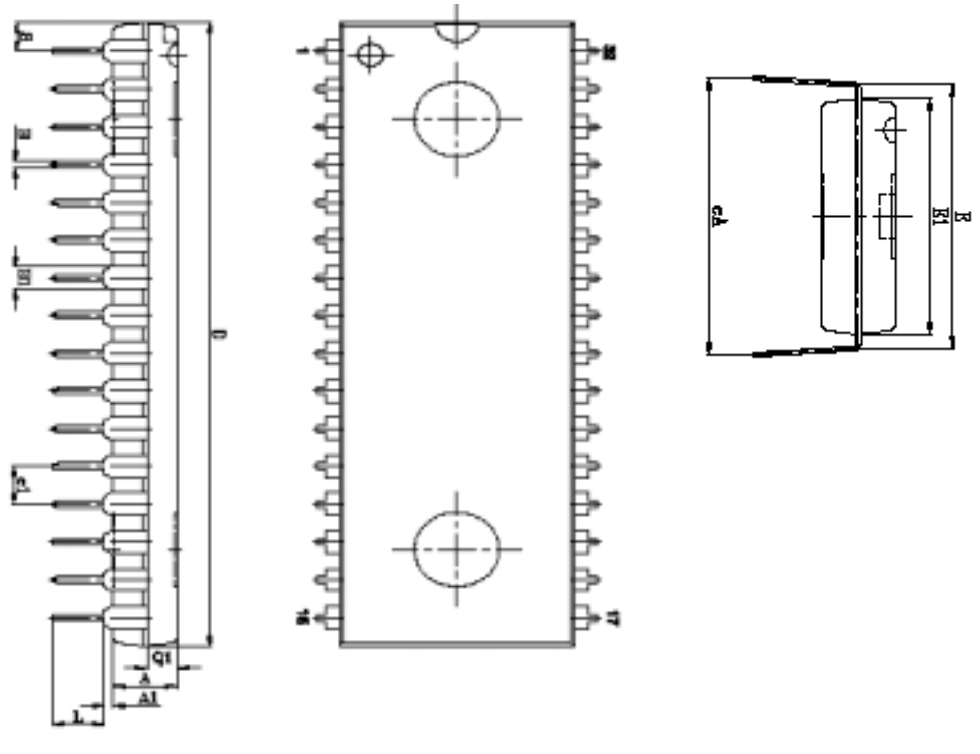


Table 8: SOP32 – 32 Lead SOP, Package Dimensions

Symbol	Mm			inches		
	Typ	Min	Max	Typ	Min	Max
A	-	-	3.00	-	-	0.118
A1	-	0.10	-	-	0.004	-
A2	2.69	2.57	2.82	0.106	0.101	0.111
b	0.41 (Ref.)			0.016 (Ref.)		
c	0.20 (Ref.)			0.008 (Ref.)		
D	20.45	20.32	20.57	0.805	0.800	0.810
E	14.12	13.87	14.38	0.556	0.546	0.566
E1	11.30	11.18	11.43	0.445	0.440	0.450
e	1.27 (Ref.)			0.050 (Ref.)		
L	0.79	0.58	0.99	0.031	0.023	0.039
ø	5º	-	-	5º	-	-

Figure 7: SOP32 – 32 Lead SOP, Package Outline

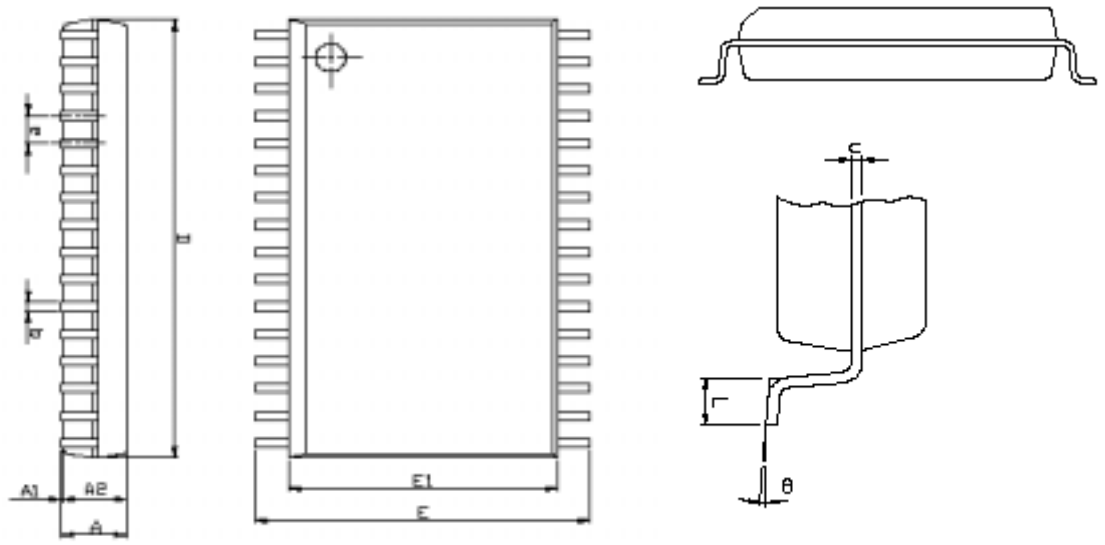


Table 9: PLCC32 – 32 Lead Plastic Leaded Chip Carrier, Package Dimensions

Symbol	Mm			inches		
	Typ	Min	Max	Typ	Min	Max
A	-	-	3.56	-	-	0.140
A1	2.16	2.03	2.29	0.085	0.080	0.090
Q1	1.27	1.22	1.32	0.050	0.048	0.052
c	0.25 (Ref.)			0.010 (Ref.)		
D	12.45	12.32	12.57	0.490	0.485	0.495
D1	11.51	11.43	11.58	0.453	0.450	0.456
D2	10.41	10.16	10.67	0.410	0.400	0.420
D3	7.62 (Ref.)			0.300 (Ref.)		
E	14.99	14.86	15.11	0.590	0.585	0.595
E1	14.05	13.97	14.12	0.553	0.550	0.556
E2	12.95	12.70	13.21	0.510	0.500	0.520
E3	10.16 (Ref.)			0.400 (Ref.)		

Figure 8: PLCC32 – 32 Lead Plastic Leaded Chip Carrier, Package Outline

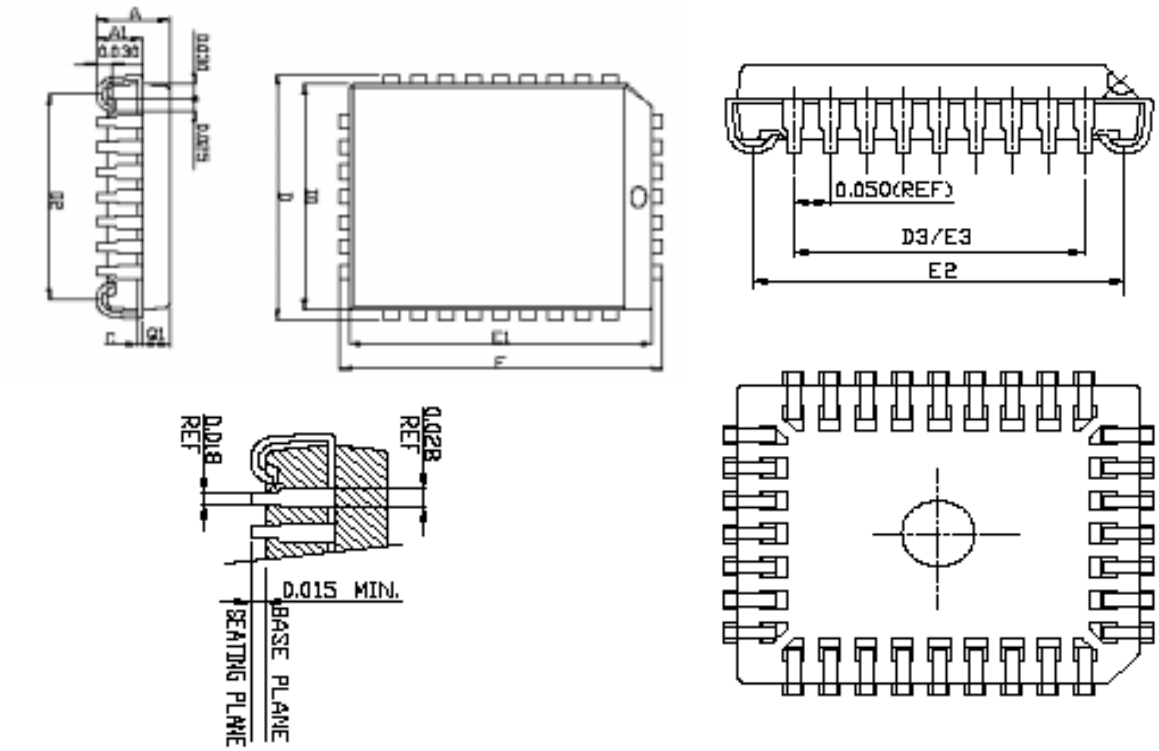
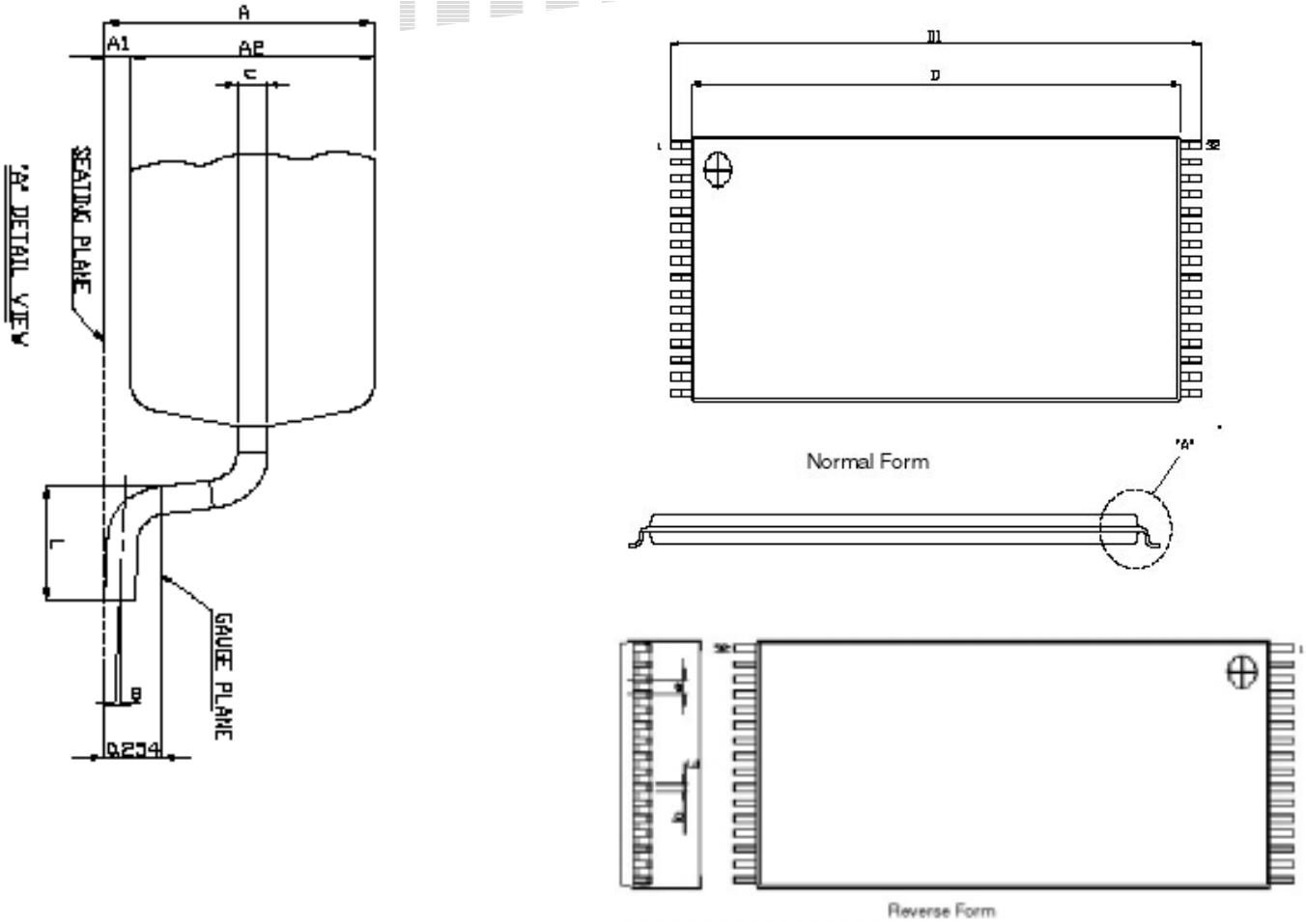


Table 10: TSOP32 – 32 Lead TSOP, Package Dimensions

Symbol	Mm			inches		
	Typ	Min	Max	Typ	Min	Max
A	-	-	1.20	-	-	0.047
A1	-	0.05	0.25	-	0.002	0.010
A2	1.00	0.95	1.05	0.039	0.037	0.041
D	18.40	18.30	18.50	0.724	0.720	0.728
D1	20.00	19.80	20.20	0.787	0.780	0.795
E	8.00	8.20	7.80	0.315	0.307	0.323
Ø	-	0º	5º	-	0º	5º
c	0.15	-	-	0.006	-	-
L	0.60	0.50	0.70	0.024	0.020	0.028
b	0.20	-	-	0.008	-	-
e	0.50 BSC.			0.197 BSC.		

Figure 9: TSOP32 – 32 Lead TSOP, Package Outline



PRODUCT ORDERING INFORMATION

AF27 C 020 -X Y Z

Device Type

AF27

Supply Voltage

C=5V
LV=3V
BV=1.8V
LC=3V ~ 5V, BC=1.8V ~ 5V, BL=1.8V ~ 3V

Device Function

020=2Mbit (256Kb x8)
2048=2Mbit (128Kb x16)

Speed

70= 70ns
90= 90ns
12= 120ns

Package

P= PDIP
S= SOIC SO= SOP
T= TSOP
TS= TSSOP
J= PLCC

Temperature

C= Commercial (0°C ~ 70°C)
I= Industrial (-40°C ~ 85°C)
M= Military (-45°C ~ 125°C)
E= Extended (Like -20°C ~ 85°C)

REVISION

Version Number	Description	Page	Date
1.0	First Preliminary Draft		8/16/02
2.0	Second Preliminary Draft	4	6/3/03

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