

Aplus Flash Technology, Inc.

Embedded Numerous-Time-Programming Flash Memory Block

1Mbit (128K bit x 8 / 64K bit x 16)

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➤ Introduction of NTP

1. General Description:

Aplus Flash Technology's NTP is a low-cost, low-voltage embedded NTP non-volatile memory IP organized as 128K bytes or 64K words (16bits) that is fully compatible with all 1.8V, 3.3V and 5.5V microprocessors. The device is using Aplus' patented proprietary design and technology to write data with a programmer approved by Aplus. A fast access time of 60ns allows the device to operate with high-speed microprocessor without wait states. For read operation, the device operates at voltages from 1.8V to 5.5V (power supply). For write operation, the device requires two external high voltages of ultrahigh VPP and ultralow VNN for cost and die size reduction. It provides word/byte program time of 10µs and chip erase time of 500ms with endurance of at least 100 cycles. The NTP is exceptionally suitable for low-voltage nonvolatile memory applications requiring infrequent writes. Manufactured with high-performance 0.18µm 2P3M CMOS Flash technology, the device provides high yield, small die size, numerous-time programming and erasing features. The NTP provides immense improvement in flexibility and performance over current nonvolatile applications that use UV-erasable OTP EPROMs and masked ROMs, while still providing the same low cost.

2. Distinctive Features & Characteristics:

- Suitable for fixed 1.8V, 3V and 5V operating supply voltages or a single wide 1.8V to 5.5V power-supply read operation
- External power supplies: ultrahigh voltage VPP and ultralow voltage VNN for patented write operation
- No internal high voltage charge pump circuits, thus reducing noise
- No internal state machine, thus reducing silicon area
- Fully compatible with 1.8V, 3.3V and 5.5V microprocessors.
- Density: 1Mbit (128K x 8bit) or (64K x 16bits)
- More die size saving for higher memory density
- High process yield: over 90%
- Access Time: 40ns @ 5V, 60ns @ 3V and 100ns @ 2.2v
- Currents: Operating: 1mA for read operation
Standby: 10µA
- Write Cycles: more than 100 cycles
- Program Time: less than 10µs per byte
- Erase Time: less than 500ms whole array
- Technology: 0.18µm 2P3M3W Flash technology.

3. NTP Embedded Numerous-Time-Programming Flash Memory Block 010/512 Related Aplus Patents

- **“Approach to provide High External Voltage for Flash Memory Erase”
U.S. Patent 06240027, granted May 29, 2001.**

- **“Approach to provide High External Voltage for Flash Memory Erase”
U.S. Patent 06166961, granted December 26, 2000.**

- **“Novel Method to turn a Flash Memory into a Versatile, low-cost NTP EEPROM” (patent pending).**

4. Block Diagram and I/O Description:

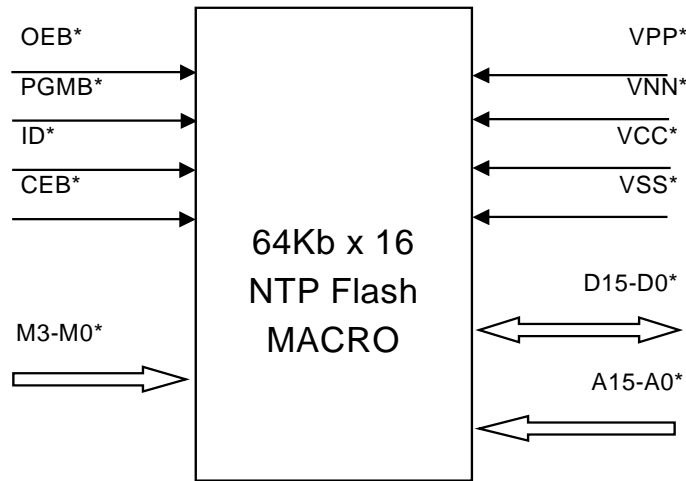


Fig. 1 Embedded NTP Block Diagram

Notes:

A signal with a star (*) means the signal is connected to external pads with multiplex function. This note is also applicable to Table 1.

Embedded NTP Interface Signals Description:

Table 1. User modes:

Connector name	Type	Description
ADDR[15:0]*	I	Provide memory addresses
DIO[15:0]*	I/O	Data input during program, data output during read, tri-state when OEB is high
OEB*	I	Output Enable, active low
CEB*	I	Chip enable, active low
PGMB*	I	Controls program, erase, or correction time.
ID*	I	ID block enable
M[3:0]*	I	Selects operation codes
VCC*	I	Power supply
VSS*	I	Ground
VPP*	I	Positive high voltage during erase, program, or correction operations
VNN*	I	Negative high voltage during erase, program or correction operations.

5.DC Specifications

Table 3. DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Battery-supply voltage	VCC	2.2	3 - 5	5.5	V
Power-supply voltage	VCC	1.8	3 - 5	5.5	V
Ground	VSS	0	0	0	V

Table 4. DC Electrical Characteristics

Parameter	Symbol	NTP010/512		Unit	Conditions
		Min.	Max.		
Operating current Read Program Erase	IDD1	-	30	mA	VCC=VCC _{Max} , OEB=VCC, Min cycle time=25MHz
		-	40	mA	
		-	40	mA	
Static Read Current	IDD2	-	1	mA	
Standby Power Supply Current	ISB	-	10	μA	CEB=VCC

Table 5. Capacitance

Parameter	Symbol	Min	Max	Unit
Address & Control Input Capacitance	Cin	-	3	pF
Data Output Pin Capacitance	Cout	-	3	pF

➤ Operating Modes Description & AC specification

1. Table 6. General Truth Table

Mode	CEB	OEB	PGMB	M[3:0]	ID	ADDR	DIN	DOUT	VPP	VNN
Standby	H	X	X	XXXX	X	X	X	HighZ	H/L	L
Read	L	L	H	LLLL	L	AIN	X	DOUT	H/L	L
Output Disable	L	H	H	LLLL	X	AIN	X	HighZ	H/L	L
Erase	L	H	L	LLHL	L	AIN	X	HighZ	VH	VL
Erase Verify	L	L	H	LLHH	L	AIN	X	HighZ	VH	VL
Program	L	H	L	LLLH	L	X	X	HighZ	VH	L

Legend: AIN=Address In, ADDR [15:0],

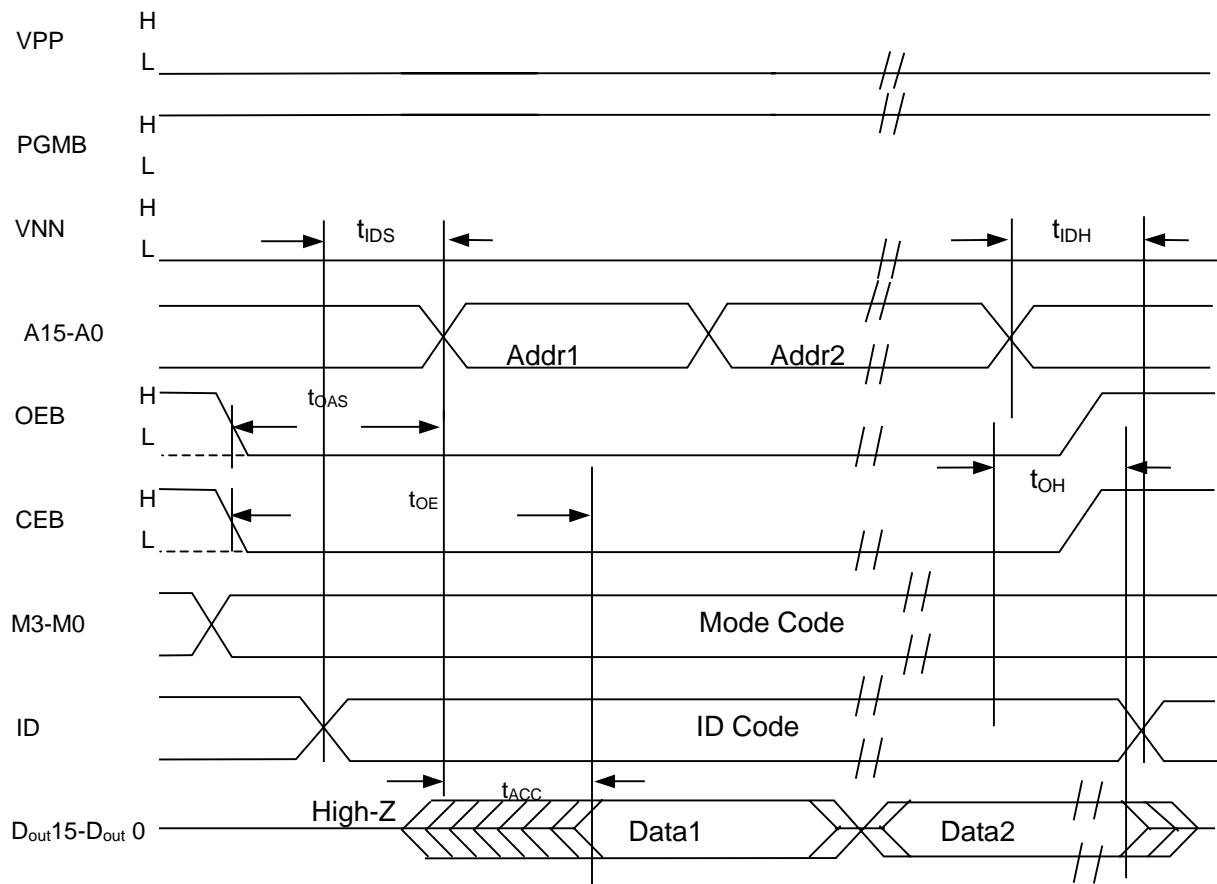
- Notes:**
1. When VNN=L and VPP= H/L it is normal mode, while VNN=L and VPP=VH it is accelerated program mode
 2. When VNN= L and VPP = H/L it is normal mode, While VNN=VL and VPP=VH it is accelerated Erase mode.

2. Table 7. General Timing AC Parameters Table (T=0C to 85C)

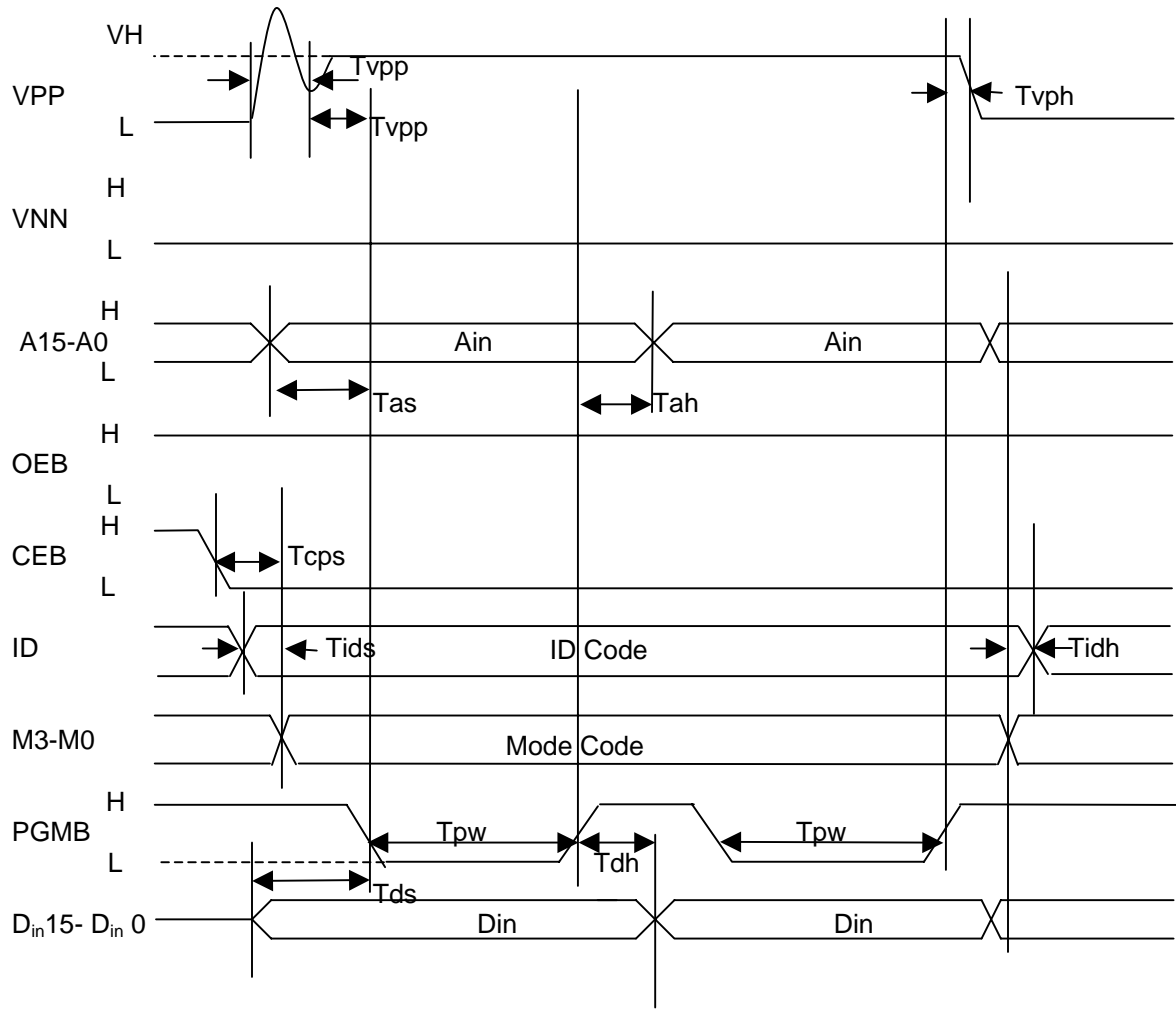
Parameter	Symbol	NTP 010		Unit
		Min	Max	
Address access time	Tacc	-	60 @ 3.0V 100 @ 2.2V	ns
OEB access time	Toas	-	30	ns
Output hold from address change time	Toh	0	-	ns
PGMB program pulse width	Tpw	10	15	μs
PGMB erase pulse width	Tew	300	350	ms
PGMB correction width	Tcw	10	15	μs
Address setup time	Tas	1	-	ns
Address hold time	Tah	1	-	ns
VPP pulse rise time	Tvps	50	-	ns
VNN pulse fall time	Tvnf	50	-	ns
VPP setup time	Tvpp	1	-	us
VPP hold time	Tvph	1	-	μs
VNN setup time	Tvns	1	-	μs
VNN hold time	Tvnh	1	-	μs
Data setup time	Tds	1	-	μs
Data hold time	Tdh	1	-	μs
VPP, VNN recovery time	Tvr	1	-	μs

3. Timing Waveforms

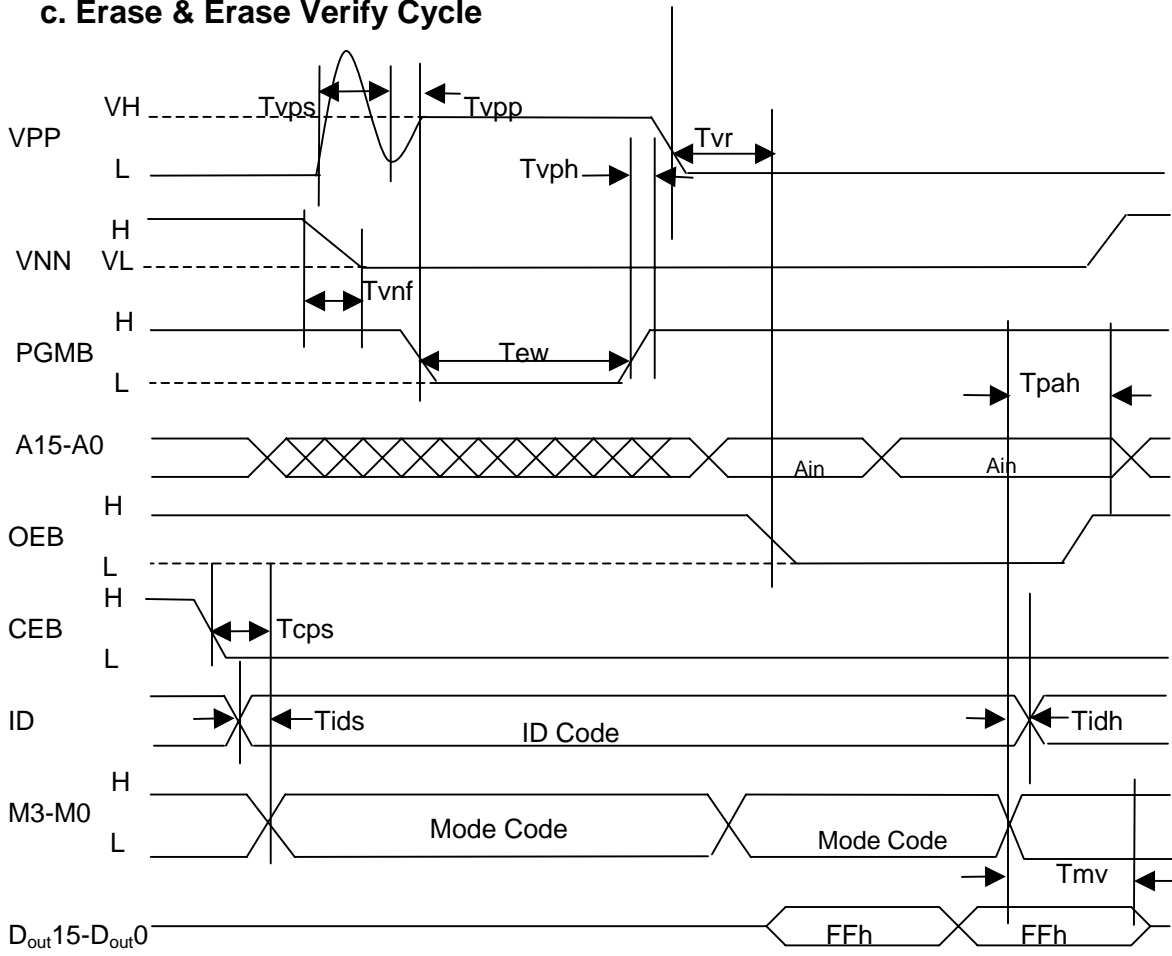
a. Read Cycle



b. Program Cycle



c. Erase & Erase Verify Cycle



REVISIONS

Version Number	Description	Page	Date
0.1	First Preliminary Draft		2/08/02
0.2	Modify block diagram and some details	2	5/28/03
0.3	The third preliminary draft		9/03/04
0.4	The fourth preliminary draft		09/15/04
0.5	The fifth draft		09/20/04

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