

## Flat Cell ROM Memory Block for Embedded Design Applications

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### Distinctive Features & Characteristics:

- Single widest Vdd operating voltages in the industry, ranging from 1.8V to 5.5V.
- 0.35um conventional BN+-bitline, flat-cell mask ROM CMOS technology for
  - Fast OS program memory:
  - Fast Read access time, faster than 80ns at 5V and 100ns at 3V for high-performance MCU applications.
  - Fast Game memory
  - Slow Speech data memory: Low cost solution for slow speech (voice) data with sampling rate ranging from 4KHZ to 8KHZ
  - Combo memory: OS code memory + Speech data memory
- Low Standby current when CEB is biased at Vdd to disable the chip.
- All data outputs are in Tri-state (High-impedance state) when either CEB or OEB at Vdd level.
- Novel low-power circuit design to completely shut off DC current consumption when any address transitions do not occur within customers' defined times.
- Novel low-power circuit design to further reduce the operating current below 20uA when operating at 32768 Hz clock operation, in battery-based consumer applications.
- Provide high design flexibility for any number of access bits in read operation (full customer design such as x8, x16 and xN per Read access).
- Small die size (@ 550um x 517um = 0.285mm<sup>2</sup> with 0.35um flat cell technology for 32K x 8).
- ROM code layer mask generation and conversion can be completely handled by Aplus (including all technical details)
- ROM code data can be forwarded to Aplus in Intel8 format or other agreed upon formats.
- ROM code data can be generated within 3 days upon data verify process
- Fast through-put from ROM-code layer generation to wafer out.
- The ROM code uses Post Poly Boron Implant
  - Without Boron data is "1"
  - With Boron data is "0"

## Description

Aplus' 0.35um 1P2M Flat-cell ROM memory block is a high-performance, highly-compact circuit block targeted for single widest Vdd operation. It can be used to store OS code for high-performance embedded CPU applications. In addition, it can be used to store the traditional speech (voice) data for slow speed application. The customized memory density varies from 8Kb to 1Mb for fast OS code and few-second to few-minute for slow voice data, covering the full range of embedded ROM applications. It is designed to be fully compatible with traditional ROM memory with a smaller die size. Fast access time of 80ns (5V) allows the device to operate with any high-speed microprocessor without additional wait state. For read operation, the memory block can operate in the widest Vdd window ranging from 1.8V to 5.5V. This flat-cell ROM design is exceptionally suitable for low-voltage, low-power consumption embedded applications. A ROM mode is provided to allow independent testing of all regular DC and AC functions of ROM from the CPU. When the memory block is disabled by CEB, a standby mode is entered with negligible DC current consumption in the circuit design.

### 32K x 8 Flat-cell OS Memory Spec Block Diagram

VDD	A14~A0
VSS	D7~D0
CEB	RESET
OEB	
OP7 ~ OP0	SAVE

## Interface Signals Description:

Connector name	Type	Description
VDD	Power	Low voltage power supply
VSS	Ground	Ground
CEB	Input	Chip Enable, active low
OEB	Input	Output Enable, active low
A14~A0	Input	Address inputs
D7~D0	I/O	Data Input/Output
RESET	Input	Reset signal; Option Bits will be latched while falling edge
OP7~OP0	Output	Customer's Defined Option Bits
SAVE	Input	Power-saving control pin

Note: Option bits are stored and defined within memory map. It may take a space of more than one address. In speech applications, it can be used to store customers' defined options such as:

- a) Level/edge trigger
- b) Rising/Falling edge trigger
- c) Repeat/Nonrepeat trigger and many others.

In Embedded CPU, the option bits can be:

- a) Security bit
- b) Trigger type
- c) Product ID
- d) Company ID and many others

## DC Operating Conditions & Temperature Range

Parameter	Symbol	Min.	Typ.	Max.	Unit
Low voltage supply	VCC	1.8	3.6	5.5	V
VSS	VSS	0	0	0	V
Ambient Temperature	Ta	0	25	70	C

## DC Electrical Characteristics

Parameter	Symbol	Typical	Maximum	Unit	Conditions
Read Current (Note1,2)	Icc		15	mA	@ 10 Mhz
Standby Current (Note 3)	Isb	10	100	uA	

**Note:**

1. The Icc is measured with OEB=Vdd. Typical specifications are for Vdd = 5V@ 25°C.
1. Isb specifications are for Vdd = 5.5V@70°C.

## Capacitance

Parameter	Symbol	Min	Maximum	Unit
Address & Control Input Capacitance	Cin	-	2	pF
Data Output Capacitance	Cout	-	2	pF

## Truth Table

Mode	OEB	RESET	CEB	D[7:0]	A[15:0]	OP7~OP0
Standby	H	L	H	High Z	X	Dout
Reset	X	H	X	High Z	X	Dout
Read	L	L	L	Dout	Ain	Dout
Latch Option Bit <sup>1</sup>	X	Rising Edge	X	X	X	Dout

### Legend:

L = Logic Low = Vss, H = Logic High = Vdd, Dout = Data Out, Ain = Address In.

### Note:

1. Address of option bits = **FFFF** or more users' defined address

## Absolute Maximum Ratings

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	VIN	-0.3V to 5.5V
Ambient Operating Temperature	Topr	-40°C to +70°C
Storage Temperature	Tstg	-65°C to +125°C

## AC Characteristics

### Flat-Cell ROM Read Operation

#### Timing AC Read Characteristics (Vcc = 5V; T = 70C)

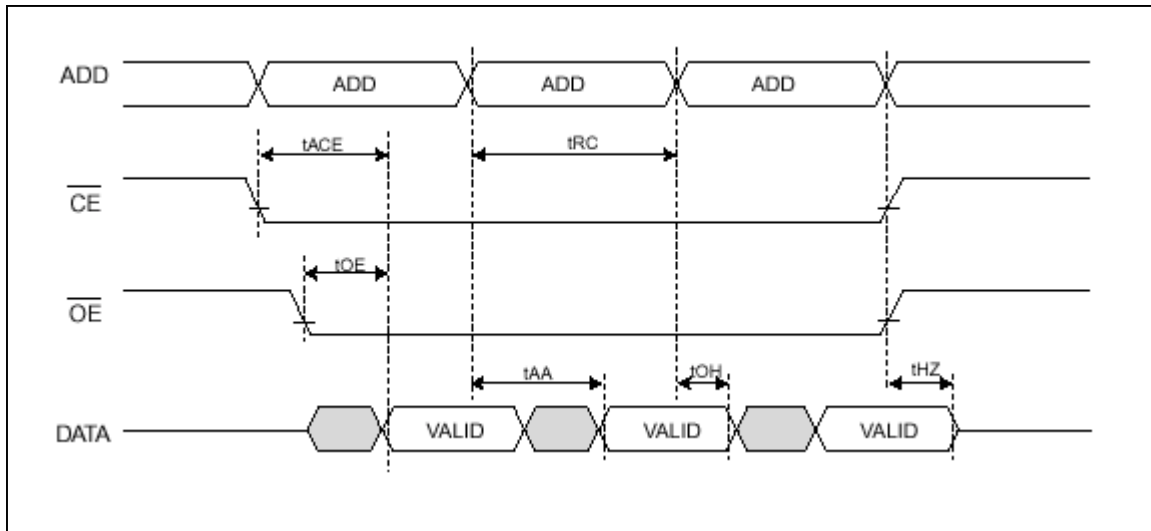
Parameter	Symbol	Min	Max	Unit
Clock Period	Tclk	25		ns
Address to Output Delay	Tacc		100	ns
CEB to P1 Setup Time	Tcp	20		ns
OEB to Output Delay	Toe		30	ns
CEB to Output High Z	Tdf		30	ns
OEB to Output High Z	Tdf		30	ns
Output Hold Time From Addresses, CEB or OEB Whichever Occurs First	Toh	0		ns

## DC Characteristics

(@V<sub>cc</sub> = 1.8V – 5.5V; T<sub>a</sub> = -40°C ~ 70°C)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	V <sub>cc</sub> - 0.2V	-	I <sub>OH</sub> = -0.4mA
Output Low Voltage	VOL	-	0.4V	I <sub>OL</sub> = 1.6mA
Input High Voltage	VIH	2.1V	V <sub>cc</sub> + 0.3V	
Input Low Voltage	VIL	-0.3V	0.4V	
Input Leakage Current	ILI	-	5μA	0V, V <sub>CC</sub>
Output Leakage Current	ILO	-	5μA	0V, V <sub>CC</sub>
Operating Current	ICC1	-	10mA	TRC = 100ns, all output open
Standby Current (CMOS)	ISTB1	10uA	100uA	CE# = VIH

## Random Read



Note:

1. CE# =  $\overline{\text{CE}}$ , OE# =  $\overline{\text{OE}}$
2. CE#, OE# are enable
3. t<sub>ACE</sub> is no longer support in the embedded design

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**REVISION**

<b>Version Number</b>	<b>Description</b>	<b>Page</b>	<b>Date</b>
0.1	First Preliminary Draft		11/15/02

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