

1KB-64KB CMOS Embedded EEPROM IP Blocks (EmbEE)

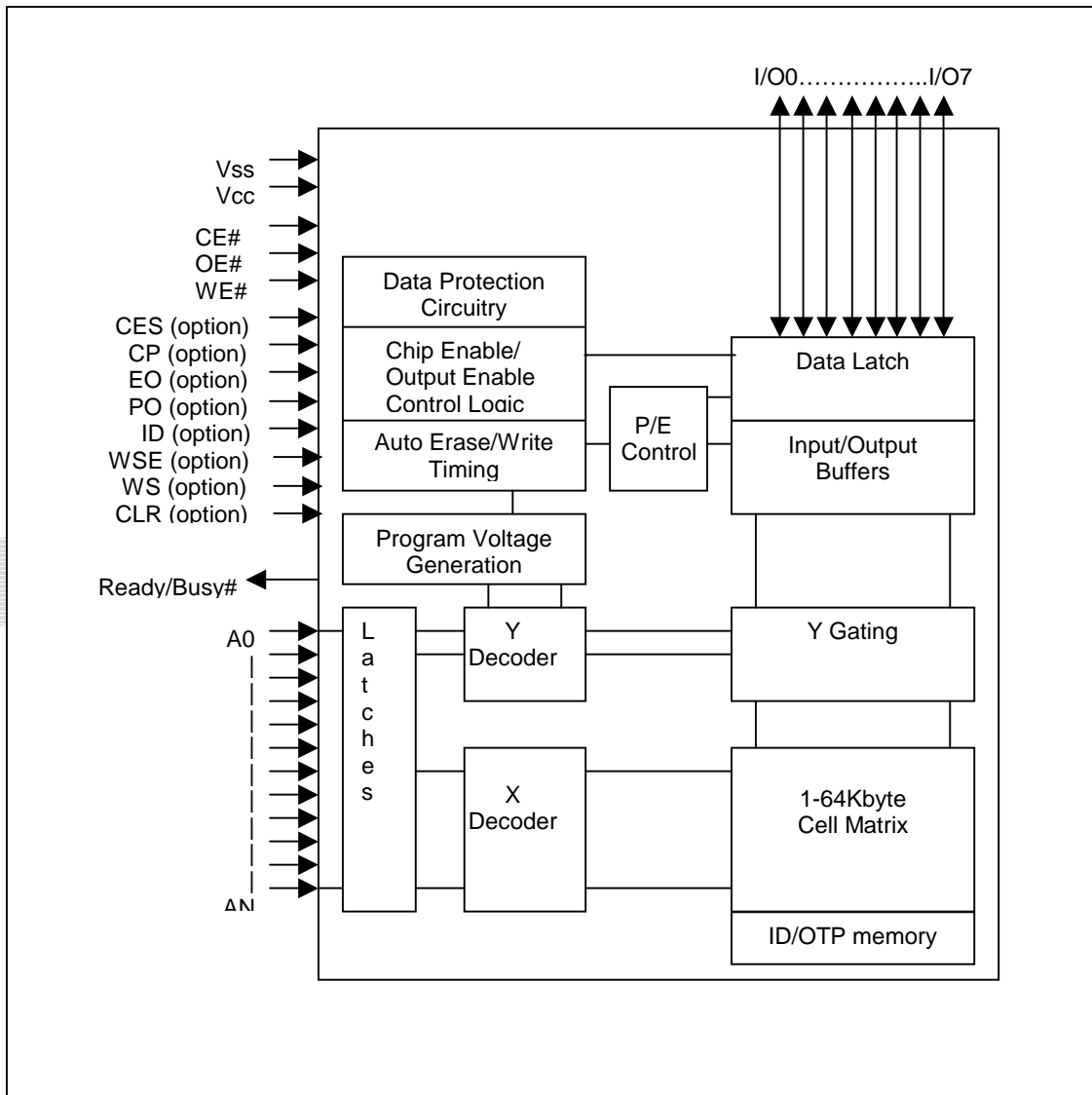
EmbEE FEATURES:

- Fast Read Access Time – 200 ns (typically 5V)
- CMOS, 2P3M, 0.35um Technology for Low Power Dissipation
 - 10mA Active
 - 10µA Standby
- Fast Write Cycle Time
 - Page Write Cycle Time – 4ms Maximum
 - 1 to 16 Byte Page Write Operation for 1KB/2KB
 - 1 to 32 Byte Page Write Operation for 4KB
 - 1 to 64 Byte Page Write Operation for 8KB/16KB/32KB
 - 1 to 128 Byte Page Write Operation for 64KB
- Data Retention >100 years
- High Endurance – Minimum 500,000 Erase/Write Cycles
- Automatic Write Operation
 - Internal Precision Control Timer
 - Auto-Clear Before Write Operation
 - On-Chip Address and Data Latches
- Ready/Busy#
- Chip Erase Operation
- Enhanced Data Protection
 - Vcc Detector
 - Pulse Filter
 - Write Inhibit
- Wide Vcc operating range (1.8 to 5.5V)
- Organized in 1K x 8 to 64K X 8 configurations
- Available for Extended Temperature Ranges:
 - Commercial: 0°C to +70°C
 - Industrial: -40°C to +85°C

DESCRIPTION

Aplus' EmbEE is a CMOS, 2P3M, 0.35um 1- 64KB non-volatile memory EEPROM. It is accessed like traditional static RAM for the read or write cycles without the need of any external components. During a "write" operation (in units of bytes), the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will enter into a busy state and automatically clear and write the latched data using Aplus' proprietary internal precision timer control. To determine when the write cycle is complete, the Ready/Busy# output monitors and flags the user upon completion. 0.35um CMOS design and processing enables this part to be used in systems where reduced power consumption, fast read speed and reliability are required. A complete family of densities is offered to provide the utmost flexibility for embedded EEPROM applications.

EmbEE BLOCK DIAGRAM



1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings*

Vcc and input voltages w.r.t. Vss	-0.6V to +6.25V
Output Voltage w.r.t. Vss	-0.6V to Vcc+0.6V
Storage temperature	-40°C to +85°C
Ambient temp. with power applied	-40°C to +85°C

*Stresses above those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device of those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 1.1: EmbEE Read/Write Operation DC Characteristic

V _{CC} = 1.8 - 5.5V Commercial (C): T _{amb} = 0°C to +70°C Industrial (I): T _{amb} = -40°C to +85°C						
Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic '1'	V _{CC}	V _{CC} -0.3	V _{CC} +1	V	
	Logic '0'	V _{SS}	-0.3	0	V	
Input Leakage	-	I _{Li}	-10	10	μA	V _{IN} = -0.1V to V _{CC} +1
Input Capacitance	-	C _{IN}	-	10	pF	V _{IN} = 0V; T _{amb} = 25°C
Output Voltages	Logic '1'	V _{CC}	V _{CC} -0.1	V _{CC}	V	I _{OH} = 2mA I _{OL} = 2mA
	Logic '0'	V _{SS}			V	
Output Leakage	-	I _{LO}	-10	10	μA	V _{OUT} = -0.1V to V _{CC} +0.1V
Output Capacitance	-	C _{OUT}	-	10	pF	V _{OUT} = 0V; T _{amb} = 25°C
Power Supply Current, Active	CMOS input	I _{CC}	-	10	mA	f = 5MHz (Note 1) V _{CC} = 5.5V
Power Supply Current, Standby (Note 2)	CMOS input	I _{CC(S)}	10	50	μA	CE# = V _{CC} , OE# = WE# = V _{CC} All other inputs equal V _{CC} or V _{SS}

Note 1: AC power supply current above 5MHz: 2mA/MHz

Note 2: In the min column 10μA is typical, not minimum. I_{cc(s)} specifications are for V_{dd} = 3.6V @ 85°C.

Table 1.2: EmbEE Read Operation AC Characteristics

AC Testing Waveform: V _{IH} = V _{CC} ; V _{IL} = 0V; V _{OH} = V _{CC} ; V _{OL} = 0V Output Load: 10 pF Input Rise and Fall Times: 20 ns Ambient Temperature: Commercial (C): T _{amb} = 0°C to +70°C Industrial (I): T _{amb} = -40°C to +85°C									
Parameter	Symbol	64/32KX8		16/8KX8		4K/2K/1KX8		Units	Conditions
		Min	Max	Min	Max	Min	Max		
Address to Output Delay	t _{ACC}	-	200	-	150	-	120	ns	OE# = CE# = V _{IL}
CE# to Output Delay	t _{CE}	-	200	-	150	-	120	ns	OE# = V _{IL}
OE# to Output Delay	t _{OE}	-	70	-	50	-	40	ns	CE# = V _{IL}
CE# or OE# High to Output Float	t _{OFF}	0	70	0	50	0	40	ns	(Note 1)
Output Hold from Address, CE# or OE#, whichever occurs first	t _{OH}	0	-	0	-	0	-	ns	(Note 1)
Endurance	-	200K	-	500K	-	1M	-	cycles	25°C

Note 1: AC power supply current above 5MHz: 2mA/MHz

Figure 1.1: EmbEE Read Waveforms

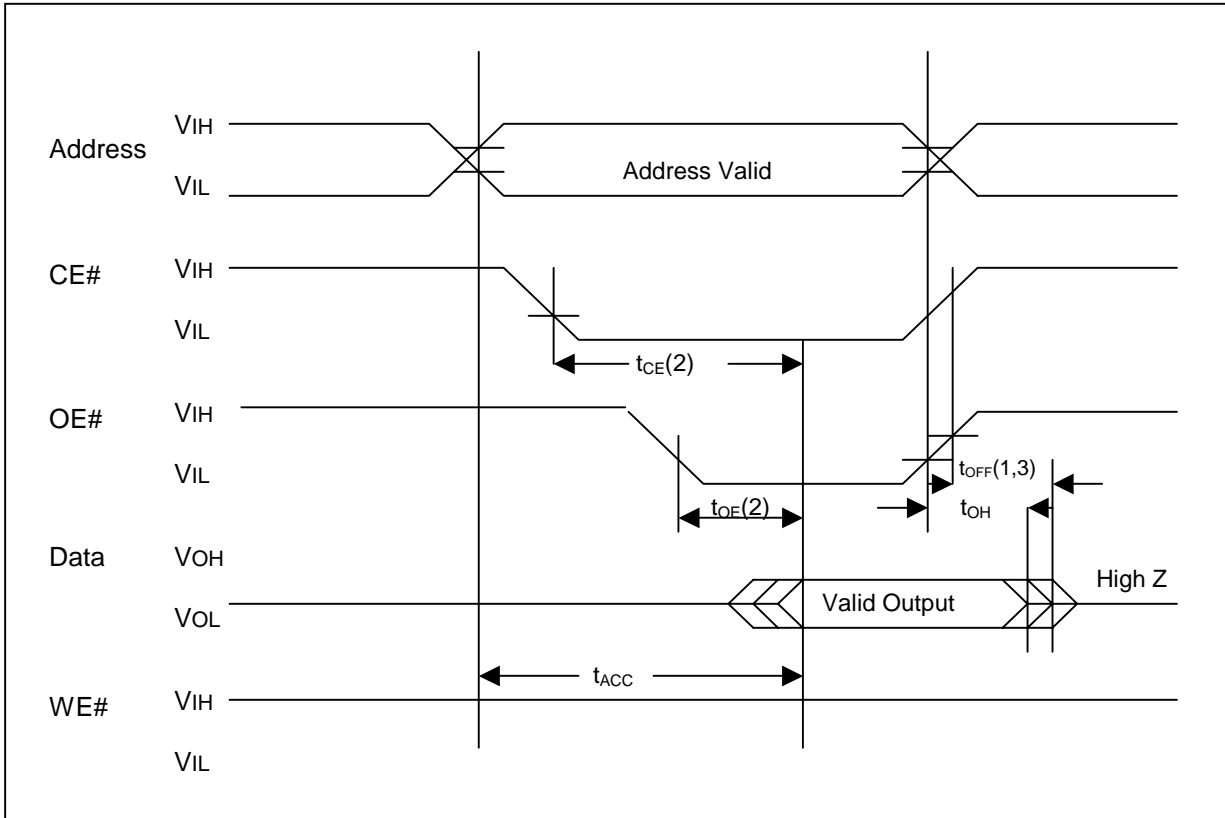


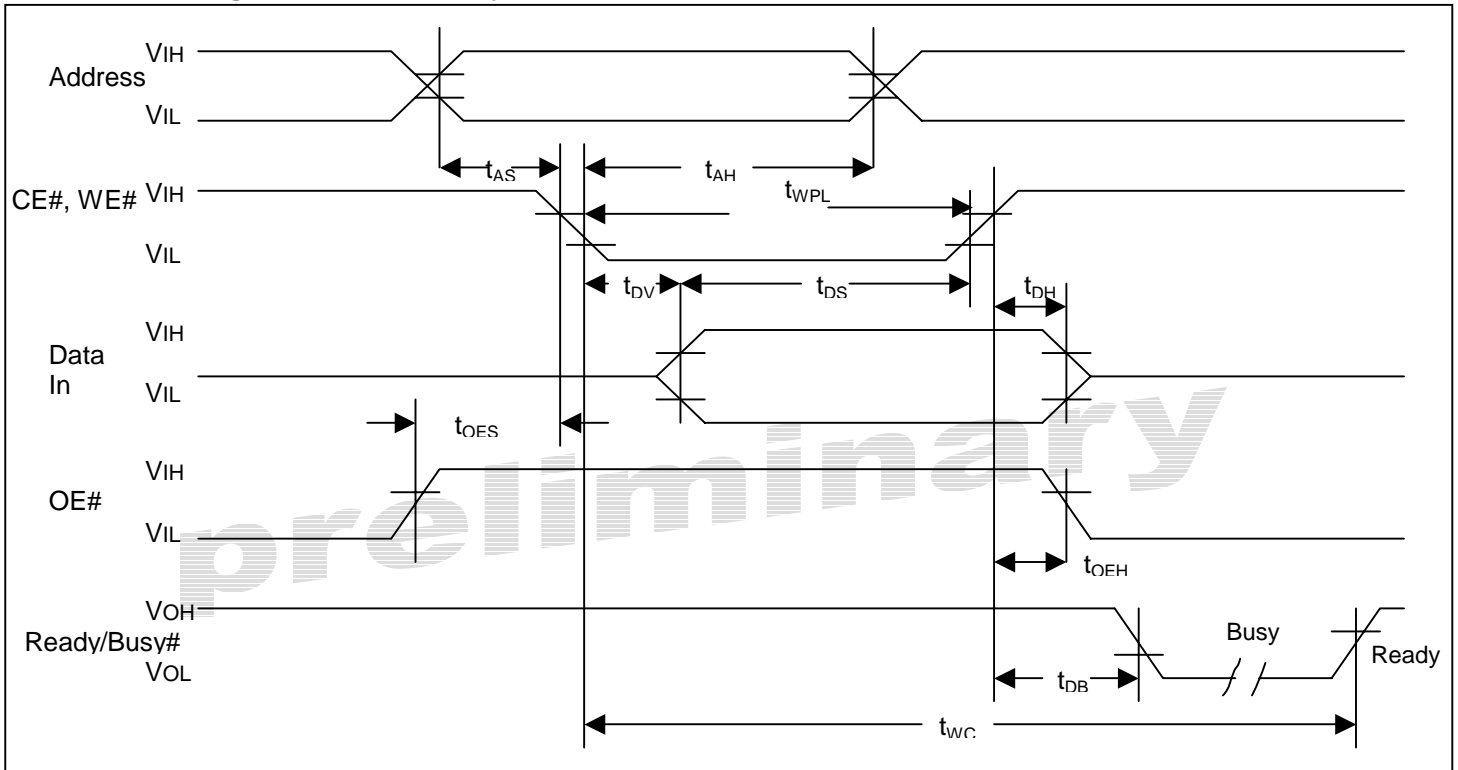
Table 1.3: EmbEE Byte Write AC Characteristics

AC Testing Waveform: $V_{IH} = V_{CC}; V_{IL} = 0V; V_{OH} = V_{CC}; V_{OL} = 0V$ Output Load: 10 pF Input Rise and Fall Times: 20 ns Ambient Temperature: Commercial (C): $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$ Industrial (I): $T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$					
Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	t_{AS}	10	-	ns	
Address Hold Time	t_{AH}	50	-	ns	
Data Set-Up Time	t_{DS}	100	-	ns	
Data Hold Time	t_{DH}	10	-	ns	
Write Pulse Width	t_{WPL}	200	-	ns	(Note 1)
Write Pulse High Time	t_{WPH}	50	-	ns	
OE Hold Time	t_{OEHL}	10	-	ns	
OE Set-Up Time	t_{OES}	10	-	ns	
Data Valid Time	t_{DV}	-	1000	ns	(Note 2)
Time to Device Busy	t_{DB}	100		μs	
Write Cycle Time	t_{WC}	-	4	ms	2ms typical
Chip Program Set-Up Time	t_{CPS}	10		ns	Option Mode
Chip Program Hold Time	t_{CPH}	10		ns	Option Mode
Erase Only Set-Up Time	t_{EOS}	10		ns	Option Mode
Erase Only Hold Time	t_{EOH}	10		ns	Option Mode
Program Only Set-Up Time	t_{POS}	10		ns	Option Mode
Program Only Hold Time	t_{POH}	10		ns	Option Mode
ID/OTP Write Set-Up Time	t_{IDS}	10		ns	Option Mode
ID/OTP Hold Time	t_{IDH}	10		ns	Option Mode
Chip Write Cycle Time	t_{CWC}	200		ms	

Note 1: A write cycle can be initiated by CE# or WE# going low, whichever occurs last. The data is latched on the positive edge WE# or CE#, whichever occurs first.

Note 2: Data must be valid within 1000ns maximum after a write cycle is initiated and must be stable at least until tDH after the positive edge of WE# or CE#, whichever occurs first.

Figure 1.2: EmbEE Byte Write Waveforms



*Data load of Page Write not shown above

Figure 1.3: EmbEE Chip Erase Waveforms (Option Mode)

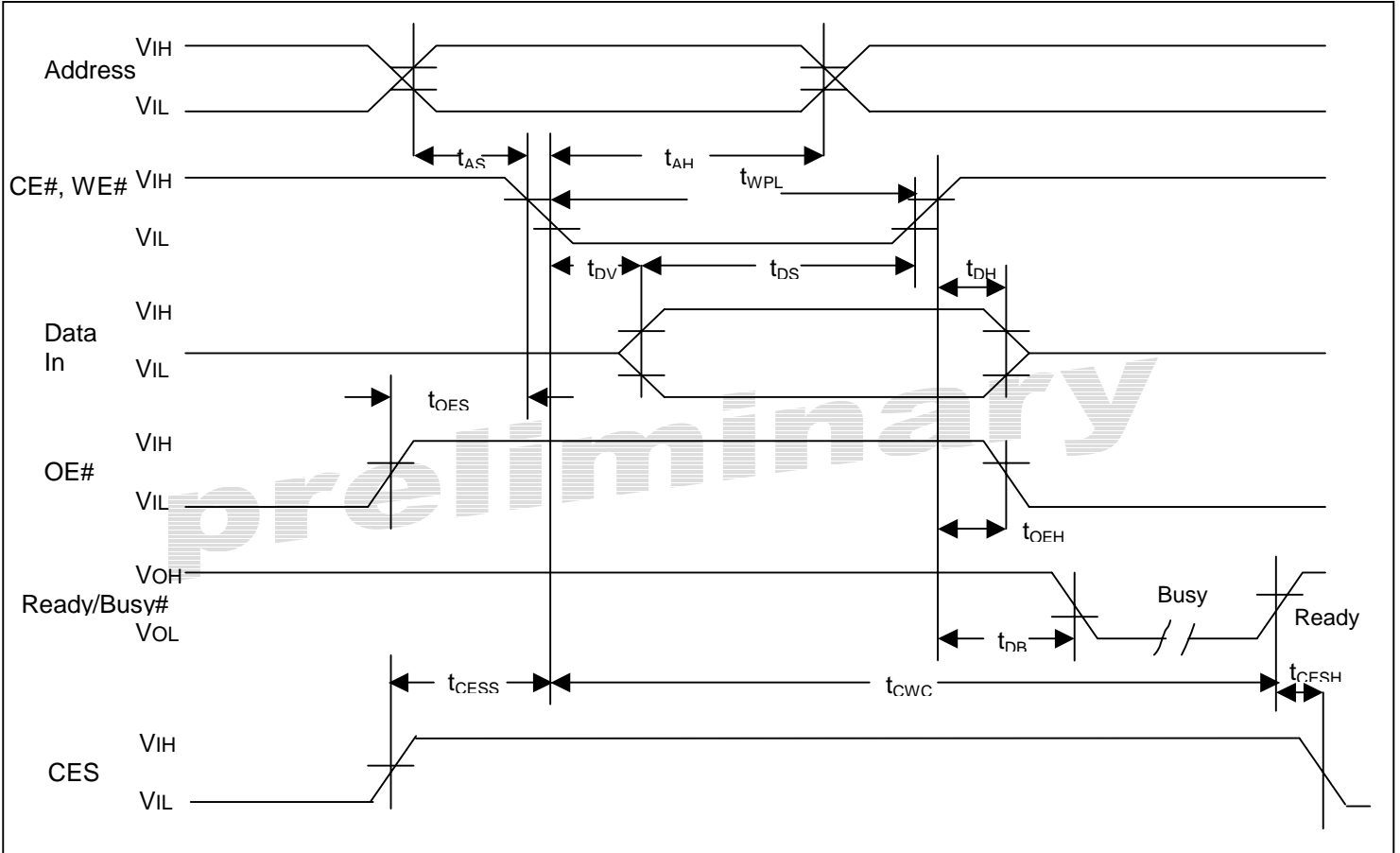


Figure 1.4: EmbEE Chip Program Waveforms (Option Mode)

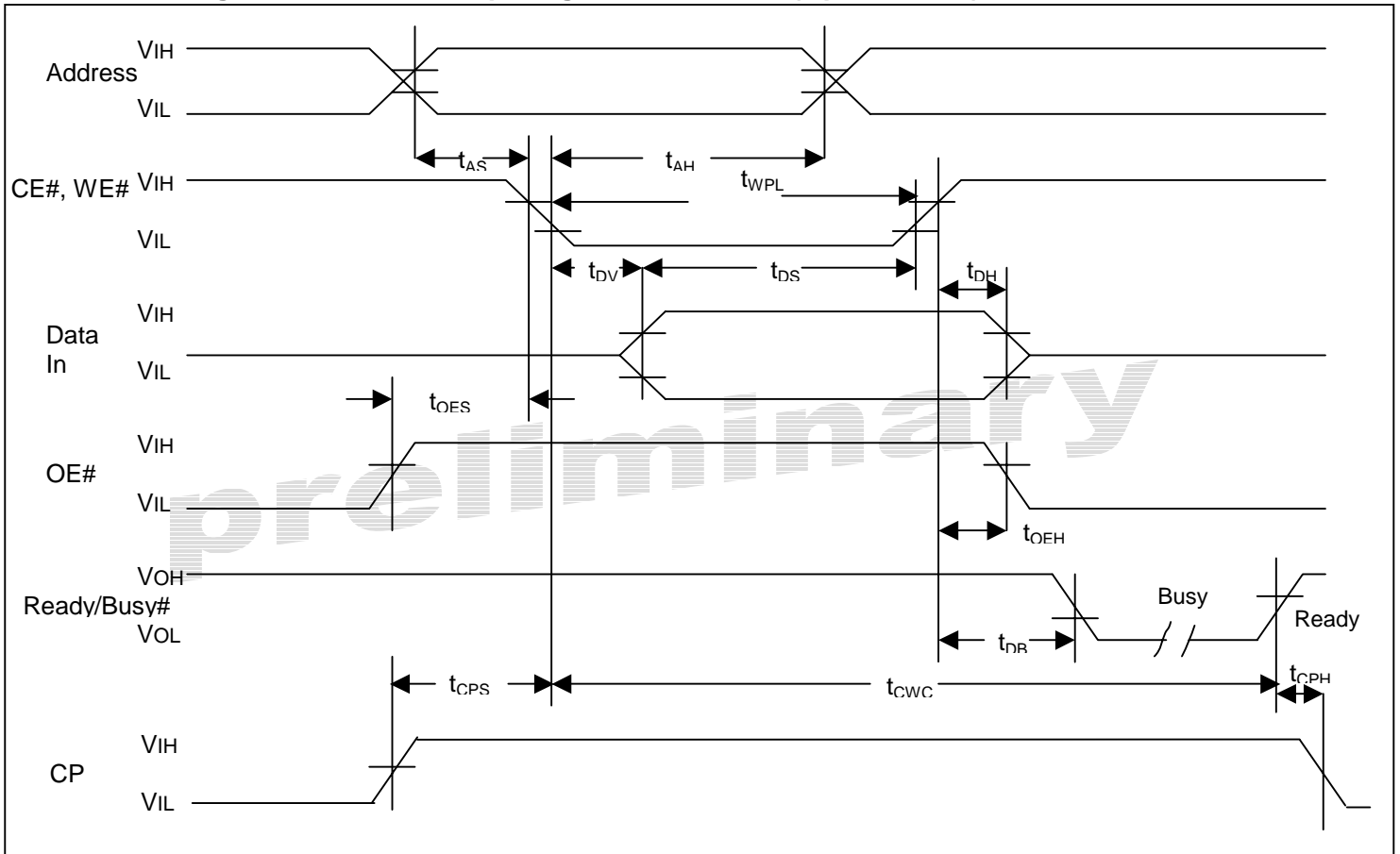


Figure 1.5: EmbEE Erase Only Waveforms (Option Mode)

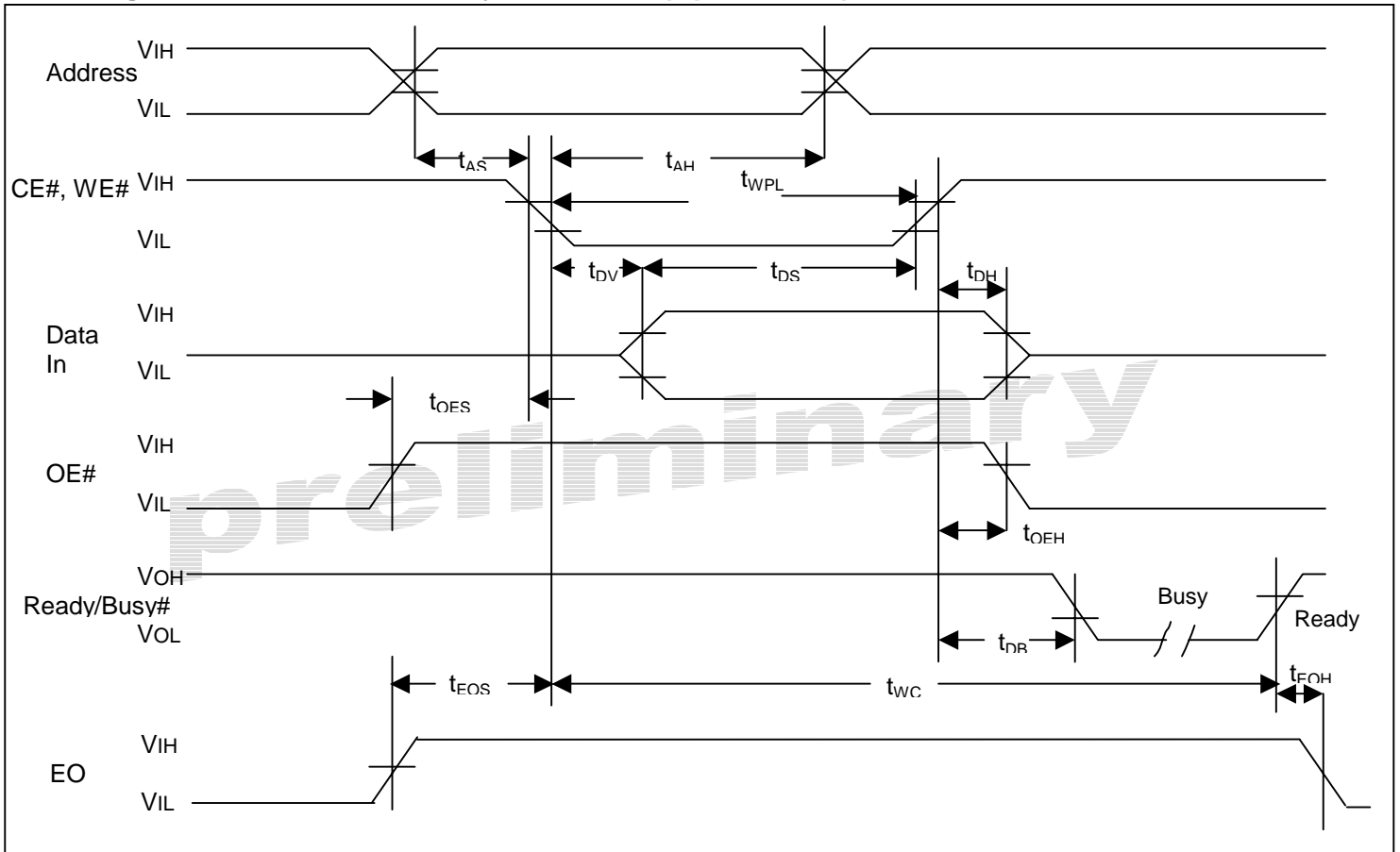


Figure 1.6: EmbEE Program Only Waveforms (Option Mode)

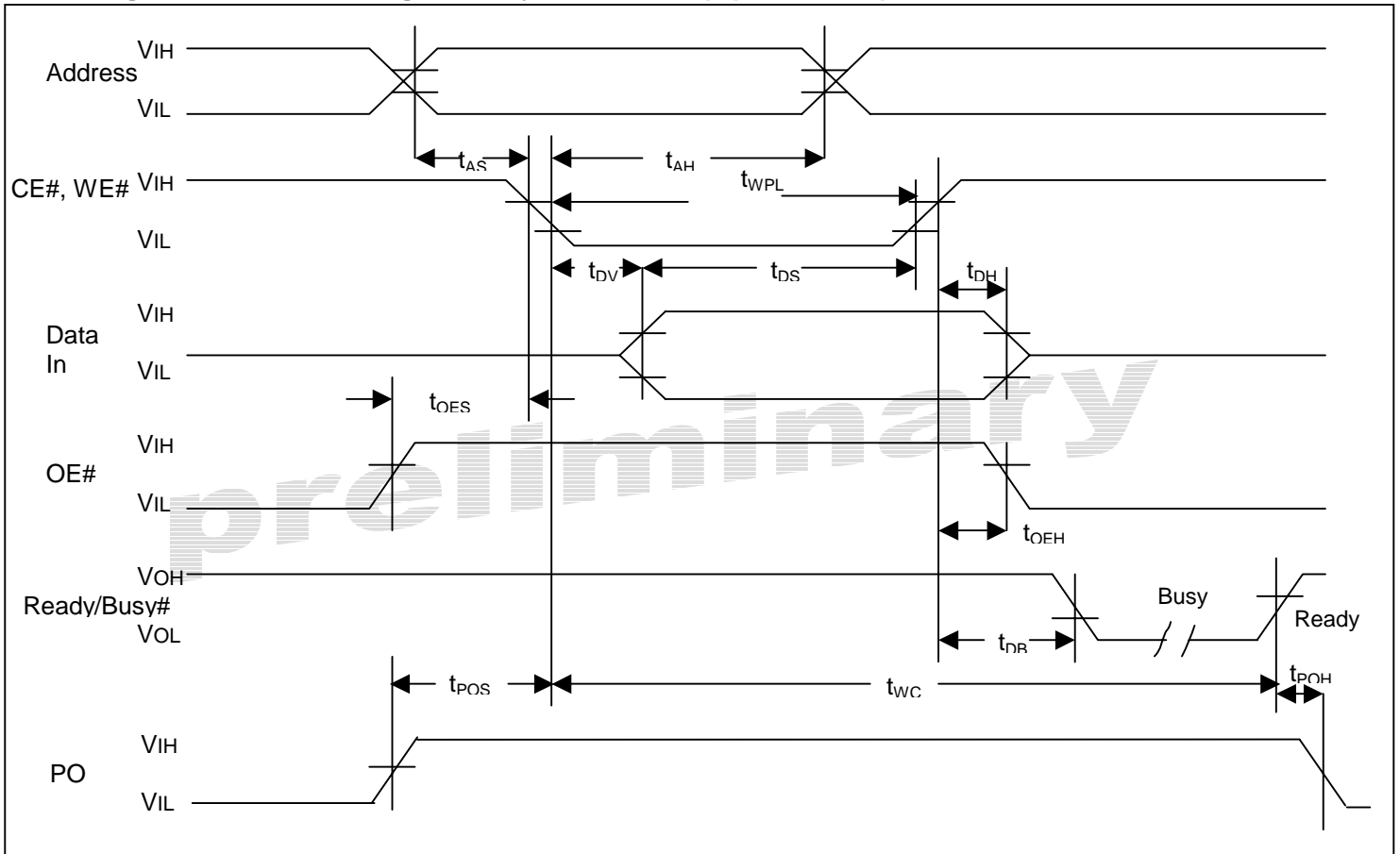
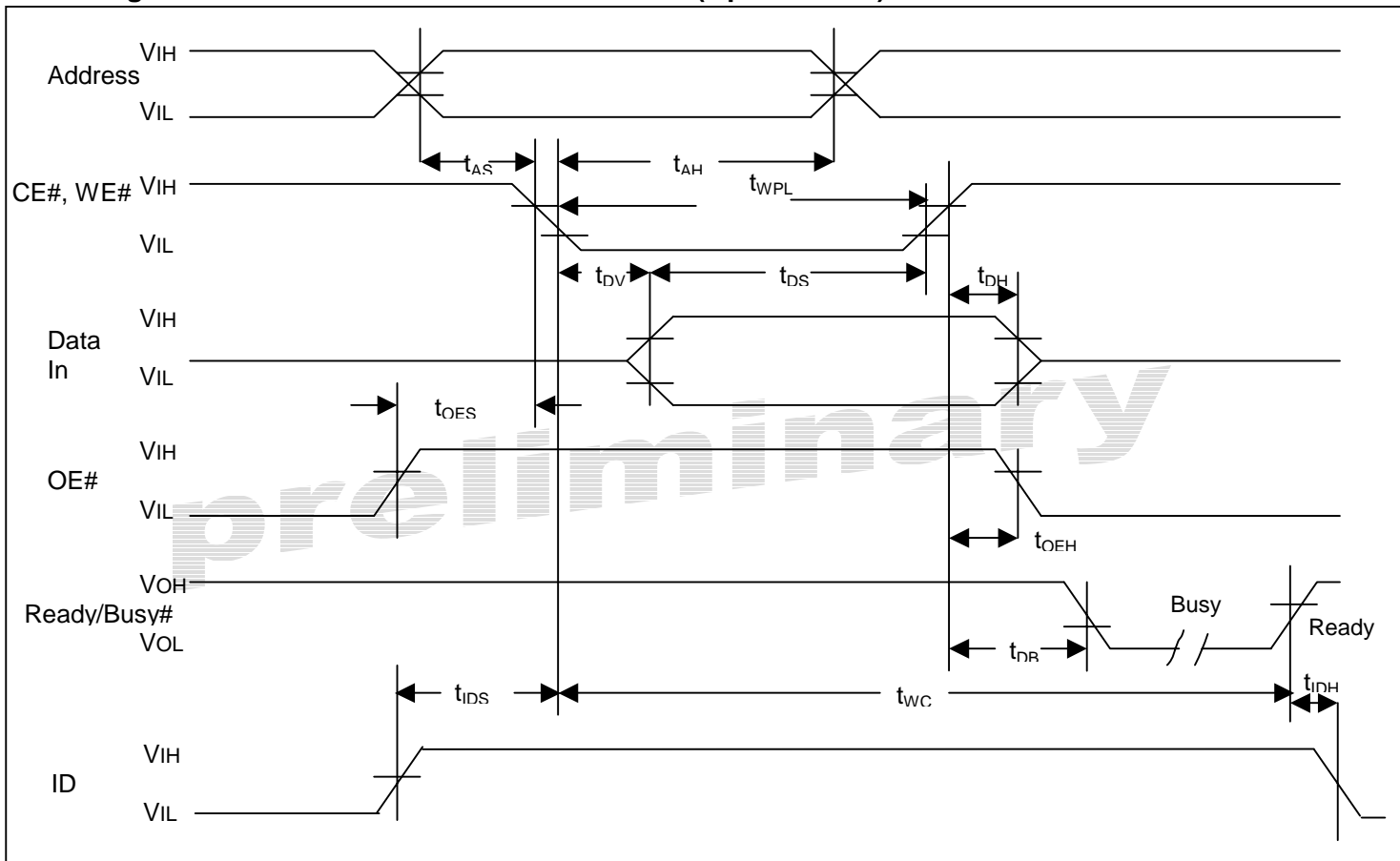


Figure 1.7: EmbEE ID/OTP Write Waveforms (Option Mode)



2.0 EmbEE DEVICE OPERATION

The EmbEE family has five basic modes and nine option modes of operations as outlined in Table 2.1 and Table 2.2:

5 basic modes – read, standby, write inhibit, byte write, and page write.

9 option modes – byte write, page write, page clear, chip erase, chip program, erase only, program only, ID/OTP read, and ID/OTP write.

The five basic modes provide users with the comprehensive functions of the conventional EEPROM. Moreover, the additional nine option modes provide users with more flexibility and more functions in system operations.

The nine option modes are enabled by the mode-select signals – WSE, WS, CLR, CES, CP, EO, PO, and ID. When one of the mode-select signals goes high, it enables the selected option mode. During the option mode operations, the read waveform and write waveform for all the other control signals remain the same as the basic modes to simplify the system controls. The option mode should be single selection. Multiple modes selected at the same time are not allowed. When the option mode-select signals all go low, it returns the chip back to normal basic mode operations. When any option mode is not

required, the corresponding mode-select signal pins can be connected to Vss to permanently disable the function.

Table 2.1: Operation Modes (Basic Signals)

Operation Mode	CE#	OE#	WE#	ADD	I/O	Ready/ Busy#
Standby	H	X	X	X	High Z	H
Read	L	L	H	AIN	DOUT	H
Write Inhibit	H	X	X	AIN		H
Write Inhibit	X	L	X	AIN		H
Write Inhibit	X	X	H	AIN		H
Byte Write (1)	L	H	L	AIN	DIN	L
Byte Write (2)	L	H	L	AIN	DIN	L
Page Write (1)	L	H	L	AIN	DIN	L
Page Write (2)	L	H	L	AIN	DIN	L
Page Clear	L	L	H	X	X	H
Chip Erase	L	H	L	X	High Z	L
Chip Program	L	H	L	X	High Z	L
Erase Only	L	H	L	AIN	DIN	L
Program Only	L	H	L	AIN	DIN	L
ID/OTP Read	L	L	H	AIN	DOUT	H
ID/OTP Write	L	H	L	AIN	DIN	L

Table 2.2: Operation Modes (Option Signals)

Operation Mode	WSE (opt)*	WS (opt)*	CLR (opt)*	CES (opt)*	CP (opt)*	EO (opt)*	PO (opt)*	ID (opt)*
Standby	X	L	L	X	X	X	X	X
Read	X	L	L	L	L	L	L	L
Write Inhibit	X	L	L	L	L	L	L	L
Write Inhibit	X	L	L	L	L	L	L	L
Write Inhibit	X	L	L	L	L	L	L	L
Byte Write (1)	L	L	L	L	L	L	L	L
Byte Write (2)	H	H	L	L	L	L	L	L
Page Write (1)	L	L	L	L	L	L	L	L
Page Write (2)	H	H	L	L	L	L	L	L
Page Clear	X	L	H	L	L	L	L	L
Chip Erase	X	L	L	H	L	L	L	L
Chip Program	X	L	L	L	H	L	L	L
Erase Only	X	L	L	L	L	H	L	L
Program Only	X	L	L	L	L	L	H	L
ID/OTP Read	X	L	L	L	L	L	L	H
ID/OTP Write	L	L	L	L	L	L	L	H

*(opt): These pins are optional for special functions. Connecting these pins to Vss can disable these functions when not used.

2.1 Read Mode

The EmbEE has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip enable (CE#) is the power control and should be used for device selection. Output Enable (OE#) is the output control and is used to gate data to the output pins independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from CE# to output (tCE). Data is available at the output tOE after the falling edge of OE#, assuming that CE# has been low and addresses have been stable for at least tACC – tOE.

2.2 Standby Mode

The EmbEE can be placed in standby mode by applying a high signal to the CE# input. When in standby mode, the outputs are in a high impedance state, independent of the OE# input.

2.3 Data Protection

In order to ensure data integrity, especially during critical power-up and power-down transitions, the following enhanced data protection circuits are incorporated:

- (1) An internal Vcc detect (2/3 of Vcc, typically) will inhibit the initiation of non-volatile programming operation when Vcc is less than the Vcc detect circuit trip.
- (2) Holding WE# or CE# high or OE# low will inhibit a write cycle during power-on and power-off (Vcc).

2.4 Byte Write

Byte write is initiated by a low pulse on the WE# input with CE# low, or a low pulse on the CE# input with WE# low. The address is latched on the falling edge of CE# or WE#, whichever occurs last. The data is latched by the rising edge of CE# or WE#, whichever occurs first. The write cycle can be initiated by two methods. The first method begins the write cycle automatically after 100us has elapsed, and the Ready/Busy# pin goes to a logic low level. Pulling the option pin WSE (Write Start Enable) to low enables this method. Pulling the option pin WSE high enables the second method. The second method starts the write cycle when the option signal WS (Write Start) is applied with a high pulse, and the Ready/Busy# pin goes to a logic low level. While the Ready/Busy# pin is low, the system bus can be used by the microprocessor host. When the Ready/Busy# signal reverts to a high logic level, the EmbEE has completed writing and can accept another cycle.

2.5 Page Write

The page-write operation of the EmbEE allows 1 to 16/32/64/128 bytes (depending on density) of data to be written into the device during a single internal write cycle. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by 1 to 15/31/63/127 additional bytes (depending on density). The write cycle can be initiated by two methods. The first method begins the write cycle automatically after 100us has elapsed. Pulling the option pin WSE (Write Start Enable) to low enables this method. Each successive byte must be written within 100us of the previous byte. If the 100us limit is exceeded, the EmbEE will cease accepting data and start the internal write cycle. Pulling the option pin WSE high enables the second method. The second method starts the write cycle when the option signal WS (Write Start) is applied with a high pulse, and the Ready/Busy# pin goes to a logic low level. The Ready/Busy# pin goes to a logic low level, indicating that the EmbEE is in a write cycle. All bytes during a page write operation must reside on the same page as defined by the address inputs. For each WE# high to low transition during the page write operation, the address inputs for the page selection must be the same. The bytes within the page may be loaded in any order and may be altered within

the same load period. Only bytes that are specified for writing will be written; unnecessary cycling of the other bytes within the page does not occur.

2.6 Page Clear

This mode allows the previously loaded data to be cleared before the write cycle is started. After byte or page data is inputted, applying a high pulse to the signal pin CLR (Clear) clears all data stored in the page buffer, abandons the write operation, and returns the chip to standby mode. Once a write cycle is started and Ready/Busy# pin goes to a logic low level, this function is ignored. This allows the user to clear unwanted loaded data and re-load the new data for a write cycle. Connecting the CLR pin to Vss can permanently disable this function when the function is not required.

2.7 Chip Erase

All data may be cleared to 1's in a chip erase cycle by following Aplus' proprietary designated waveforms as shown in FIG.1.3. This procedure clears all data in memory within a pre-determined time. To enable the chip erase operation, the chip-erase mode select signal CES has to be pulled to logic high and remain high until the entire chip-erase operation is complete. The chip erase operation is initiated by using the same waveform as byte-write operation shown in FIG.1.2, except the input address and data are not care in this mode. The chip erase operation is initiated by a low pulse on the WE# input with CE# low, or a low pulse on the CE# input with WE# low. The address is latched on the falling edge of CE# or WE#, whichever occurs first. The data is latched by the rising edge of CE# or WE#, whichever occurs first. The chip erase cycle begins after 100us has elapsed, and the Ready/Busy# pin goes to a logic low level. While the Ready/Busy# pin is low, the system bus can be used by the microprocessor host. When the Ready/Busy# signal reverts to a high logic level, the EmbEE has completed chip erase. The system can pull low the CES to return the chip back to normal mode and start another cycle. Connecting the CES pin to Vss can permanently disable this function when the function is not required.

2.8 Chip Program

All data may be programmed to 0's in a chip program cycle by following Aplus' proprietary designated waveforms as shown in FIG.1.4. This procedure programs all data in memory within a pre-determined time. To enable the chip program operation, the chip-program mode select signal CP has to be pulled to logic high and remain high until the entire chip-program operation is complete. The chip program operation is initiated by using the same waveform as byte-write operation shown in FIG.1.2, except the input address and data are not care in this mode. The chip program operation is initiated by a low pulse on the WE# input with CE# low, or a low pulse on the CE# input with WE# low. The address is latched on the falling edge of CE# or WE#, whichever occurs last. The data is latched by the rising edge of CE# or WE#, whichever occurs first. The chip program cycle begins after 100us has elapsed, and the Ready/Busy# pin goes to a logic low level. While the Ready/Busy# pin is low, the system bus can be used by the microprocessor host. When the Ready/Busy# signal reverts to a high logic level, the EmbEE has completed chip program. The system can pull low the CP to return the chip back to normal mode and start another cycle. Connecting the CP pin to Vss can permanently disable this function when the function is not required.

2.8 Erase Only

This mode allows the data of the selected bytes to be changed from '0's to '1's only. When the EO pin is high, it disables the internal program operation of the EEPROM so the selected bytes can only be changed from '0' to '1' in the same manner as the regular write operation waveform. The waveform for controlling the erase only operation is shown in FIG.1.5. Connecting the EO pin to Vss can disable this function when the function is not required.

2.9 Program Only

This mode allows the data of the selected bytes to be changed from '1's to '0's only. When the PO pin is high, it disables the internal erase operation of the EEPROM so the selected bytes can only be changed from '1' to '0' in the same manner as the regular write operation waveform. The waveform for controlling the program only operation is shown in FIG.1.6. Connecting the PO pin to Vss can disable this function when the function is not required.

3.0 ID/OTP Mode

An extra page of 16/32/64/128 bytes (depending on density) of EEPROM memory is available to the user for device identification or other one-time-programming purposes. When ID pin is high, the additional bytes may be written to or read from in the same manner as the regular memory array. The waveform for controlling the ID/OTP-write operation is shown in FIG.1.7. Connecting the ID pin to Vss can disable this function when the function is not required.

3.1 Built-In Testability

The EmbEE has a versatile built-in testability. All the functions plus seven EEPROM specific test modes are accessible by external tester control. The test port interface is multiplexed with the embedded system pins so no extra pin is required. The test function interface requires only six pins to support those low pin count applications.

preliminary

REVISIONS

Version Number	Description	Page	Date
0.1	First Preliminary Draft		11/22/02
0.2	Second Preliminary Draft	5-14	12/13/02
0.3	Third Preliminary Draft	2, 11-15	1/17/03

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