

## **OTP EPROM Memory Block for Embedded Design Applications (0.35 EmbOTP)**

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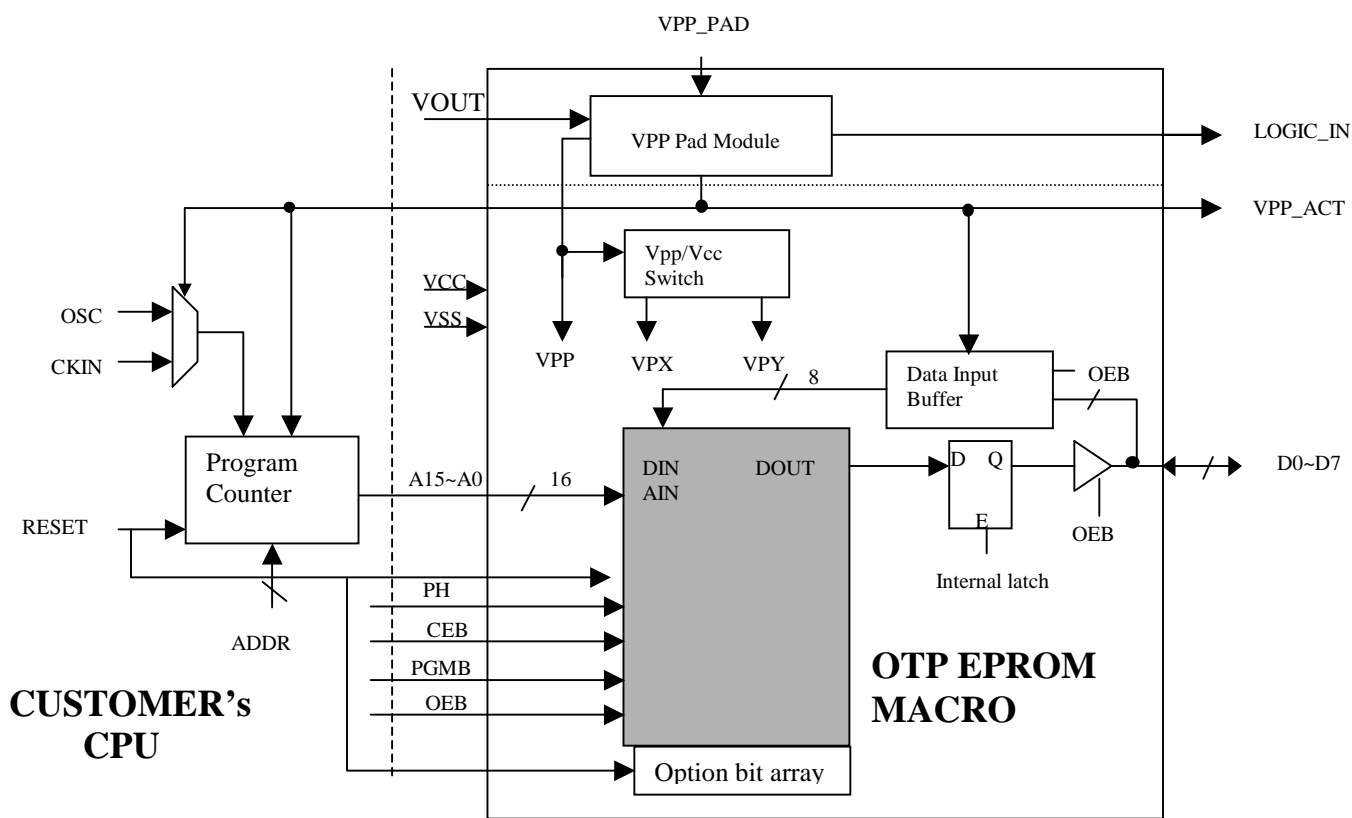
### **Distinctive Features & Characteristics:**

- Operating voltages ranging from 2.7V to 3.6V.
- Fast Read access time, faster than 80ns at 3V and 100ns at 2.7V.
- Low Standby current when CEB is biased at Vcc to disable the chip.
- All outputs are in Tri-state (High-impedance state) when either CEB or OEB at Vcc level.
- Novel low-power circuit design to completely shut off DC current consumption when any address transitions do not occur within 1us, typically.
- Novel low-power circuit design to further reduce the operating current below 10uA when operating at 32768 Hz clock operation, in battery-based consumer applications.
- Provide high design flexibility for any number of access bits in read operation (full customer design such as x8, x16 and xN per Read access).
- Small die size
- High UV Erase yield, UV Erase uniformity and UV Erase integrity have been well designed-in for memory densities ranging from 8Kb to 4Mb.
- VPP programming voltage of 12V or below is designed to be fully compatible with the traditional EPROM programmer, to achieve larger breakdown margin.
- VPP pin can also be used to apply Vcc or ground for Read operation, without requiring additional pad.
- Unique circuit design to achieve high programming yield for high Vcc applications.
- Fast program time: Less than 100us per word (16-bit).

### **Description**

Aplus' 0.35um 2P2M OTP memory block is a high-performance circuit block targeted for Vcc 2.7V to 3.6V operation. The memory density varies from 8Kb to 4Mb to cover the full range of Embedded OTP applications. It's been designed to be fully compatible with the traditional OTP memory. Fast access time of 80ns (3V) allows the device to operate with any high-speed microprocessor without additional wait state. For read operation, the memory block can operate in window ranging from 2.7V to 3.6V. This OTP design is exceptionally suitable for low-voltage, low-power consumption embedded applications. An OTP mode is provided for all regular DC and AC function tests even after the sealing of the package. A security mode to protect the on-chip stored code data is also provided. When the memory block is disabled by CEB, a standby mode is entered with zero DC current consumption.

## Standard 64K x 8 OTP EPROM Macro Spec: Embedded OTP Block Diagram



**Table 1. Interface Signals Description:**

Connector name	Type	Description
VPP	Power	High voltage power supply
VCC	Power	Low voltage power supply
VSS	Ground	Ground
CEB	Input	Chip Enable, active low
OEB	Input	Output Enable, active low
PGMB	Input	Program strobe, active low to control program time
A15~A0	Input	Address inputs
D7~D0	I/O	Data Input/Output
VPP_ACT	Output	VPP_ACT=1 while VPP is applied to 12V
PH	Input	Customer's synchronous signal for saving power in the application during low frequency operation
LOGIC_IN	Output	Customer's defined logic input which can be multiplexed with VPP during VPP=12V whether it is at logic '0' or '1'. It performs as normal logic when VPP=Vcc or Vss.
VOUT	Input	Customer's defined output which can be multiplexed with VPP and has pull-down function.
RESET	Input	Program and Read Option Bit, high active

**Table 2. DC Operating Conditions & Temperature Range**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Low voltage supply	VCC	2.7	3.0	3.6	V	Read Mode: VPP=VCC or VSS
High voltage supply	VPP	--	12	--	V	Program Mode: VCC = 6V
VSS	VSS	0	0	0	V	
Ambient Temperature	Ta	0	25	70	C	

**Notes:**

1. Vcc must be applied before or simultaneous with VPP and removed after or simultaneous with VPP.
2. During programming operation, a 0.1uF capacitor is required across VPP and ground to suppress spurious voltage transients which may damage the device.

**DC Electrical Characteristics (Ta=0° ~70°C)**

Parameter	Symbol	Typical	Maximum	Unit	Conditions
Read Current (Note 1)	Icc	4	8	mA	@ 4MHz Read Cycle
Program Current	Ipp	20	40	mA	VPP=12V, Vcc=6V
Standby Current	ISB	10	100*	uA	*Vcc=max



**Notes:**

1. The Icc is measured with OEB=Vcc. Typical specifications are for Vcc = [3.0V@25C](#).

**Capacitance**

Parameter	Symbol	Min	Maximum	Unit
Address & Control Input Capacitance	Cin	-	3	pF
Data Output Capacitance	Cout	-	3	pF

**Truth Table**

Mode	OEB	PGMB	PH	RESET	CEB	VPP	D[7:0]	A[15:0]
Standby	X	X	X	L	H	H/L	High Z	H/L
Read	L	H		L	L	H/L	Dout	Ain
Program	H	L	L	L	L	VH	Din	Ain
Program Verify	L	H	L	L	L	VH	Dout	Ain
Program Inhibit	X	X	X	L	H	VH	High Z	H/L
Latch Test Mode <sup>1</sup>	H	H	L	L	Falling Edge	VH	Din	H/L
Option Bit Program <sup>2</sup>	H	L	L	L	L	VH	Din	Ain
Option Bit Verify	L	H	L	L	L	VH	Dout	Ain
Option Bit Read	L	H		H	L	H/L	Dout	Ain
OTP read	L	H	L	L	L	VH	Dout	Ain

**Legend:**

L = Logic Low = Vss, H = Logic High = Vcc, VH = 12+- 0.5V, X = Don't Care, Din = Data In, Dout = Data Out, Ain = Address In, H/L=Logic High or Logic Low

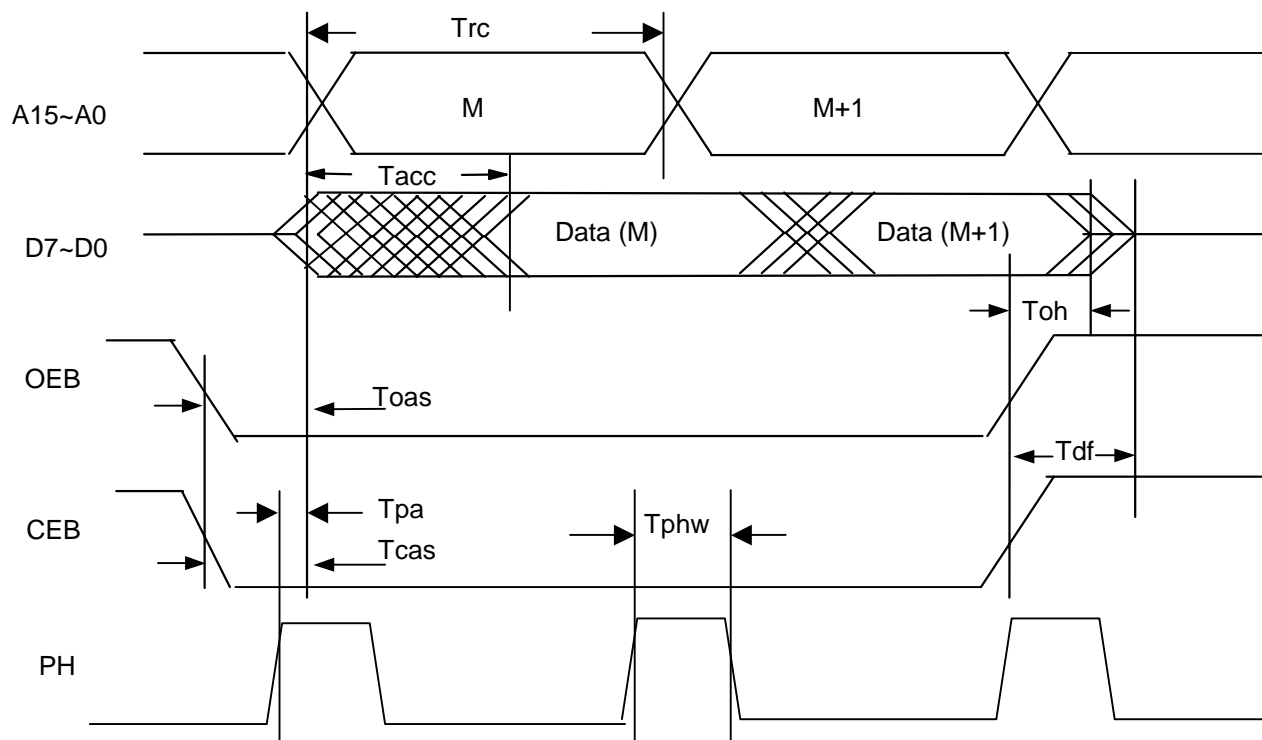
**Note:**

1. Program Mode: D[7:0] = 00H  
OTP Read Mode: D[7:0]=01H,
2. Option Bit Program Mode: d[7:0] = 02H

## OTP EPROM Read Operation

### Timing AC Read Characteristics ( $V_{cc}=3.0V$ ; $T_a=25^{\circ}C$ )

Parameter	Symbol	Min	Max	Unit
Read Cycle Time	Trc	80		ns
PH to Address Valid Time Delay	Tpa		5	ns
High Pulse Width of PH	Tphw	20		ns
Address to Output Delay	Tacc		80	ns
CEB to Address Valid Setup Time	Tcas	Trc		ns
OEB to Address Valid Setup Time	Toas	Trc		ns
CEB to Output High Z	Tdf		15	ns
OEB to Output High Z	Tdf		15	ns
Output Hold Time From Addresses, CEB or OEB Whichever Occurs First	Toh	0		ns

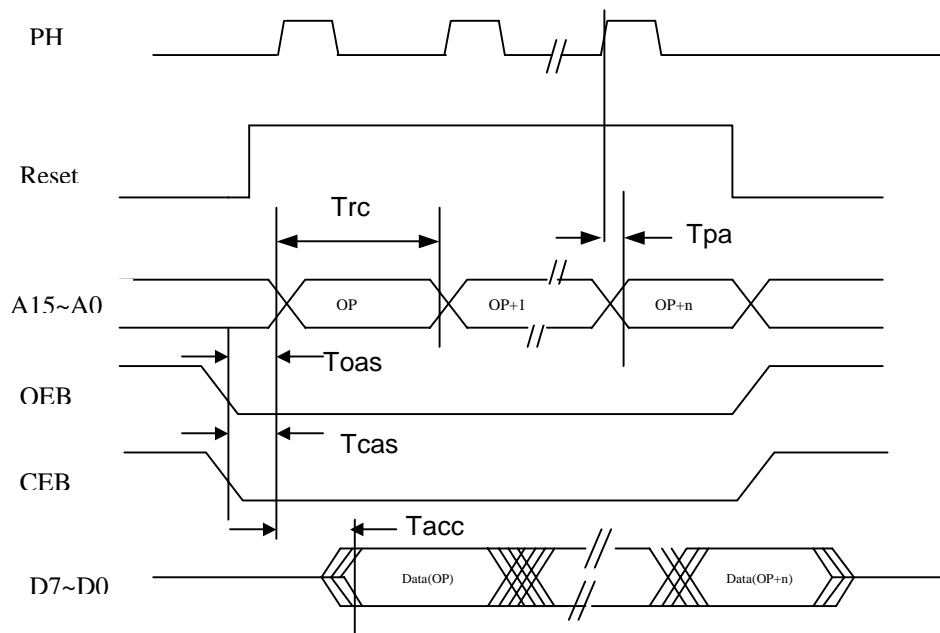


**Fig.1 Read Operations Timing**

### Read Mode:

To obtain data at the OTP EPROM macro outputs, Chip Enable (CEB) and Output Enable (OEB) must be driven low with at least 1 read clock cycle time as a dummy cycle. This dummy read cycle time is designed to ensure in advance the stability of the internal bias circuit of the OTP EPROM for the application by using a high frequency system clock. Note that each read clock cycle is synchronized with PH. This means that each transient address occurs after each PH's rising edge. In each read

clock cycle, the user can define as many phases as they want. When address is kept stable for  $T_{acc}$ , the user can read out the data in the remaining read clock cycle and latch data at a certain phase. CEB controls PGMB & OEB to select the OTP EPROM macro. OEB enables the OTP EPROM macro to output data. In some applications, by using a low frequency system clock, the auto sleep mode will be automatically enabled to minimize the power consumption in the OTP EPROM macro. Owing to each PH's rising edge, the internal delay will be activated for 1~2us and the data will be latched right after reaching the delay time. During the sleep period, data is always available to the system as long as CEB and OEB are driven low. For example, assuming that the read cycle time is 32us and the delay time is 2us, the total power saved can be up to 15/16 (93.75%). On the contrary, in the application using high frequency system clock, the sensed data in OTP EPROM macro is always transparent to the data bus as long as CEB & OEB are driven low.



**Fig.2 Option Bits Read Operations Timing**

### Option Bits Read Mode:

Option bits are located in other extra memory arrays, usually one full row, and Aplus reserves the last byte of this row for special use. Whether performing a program, program verify, OTP read or normal read operations, they are treated the same as the other normal OTP EPROM cells. Below, there is one explanatory example described with the timing waveform above.

At accessing option bits mode, customer can issue "RESET" signal and the associated "OEB" & "CEB" to read out the option bits byte by byte while address counter is incremented by "CKIN". For example, if the option bit number is 48, there will be 6 "CKIN" clocks and 6 "ADDR" valued from 0 to 5 during "RESET" period. The read

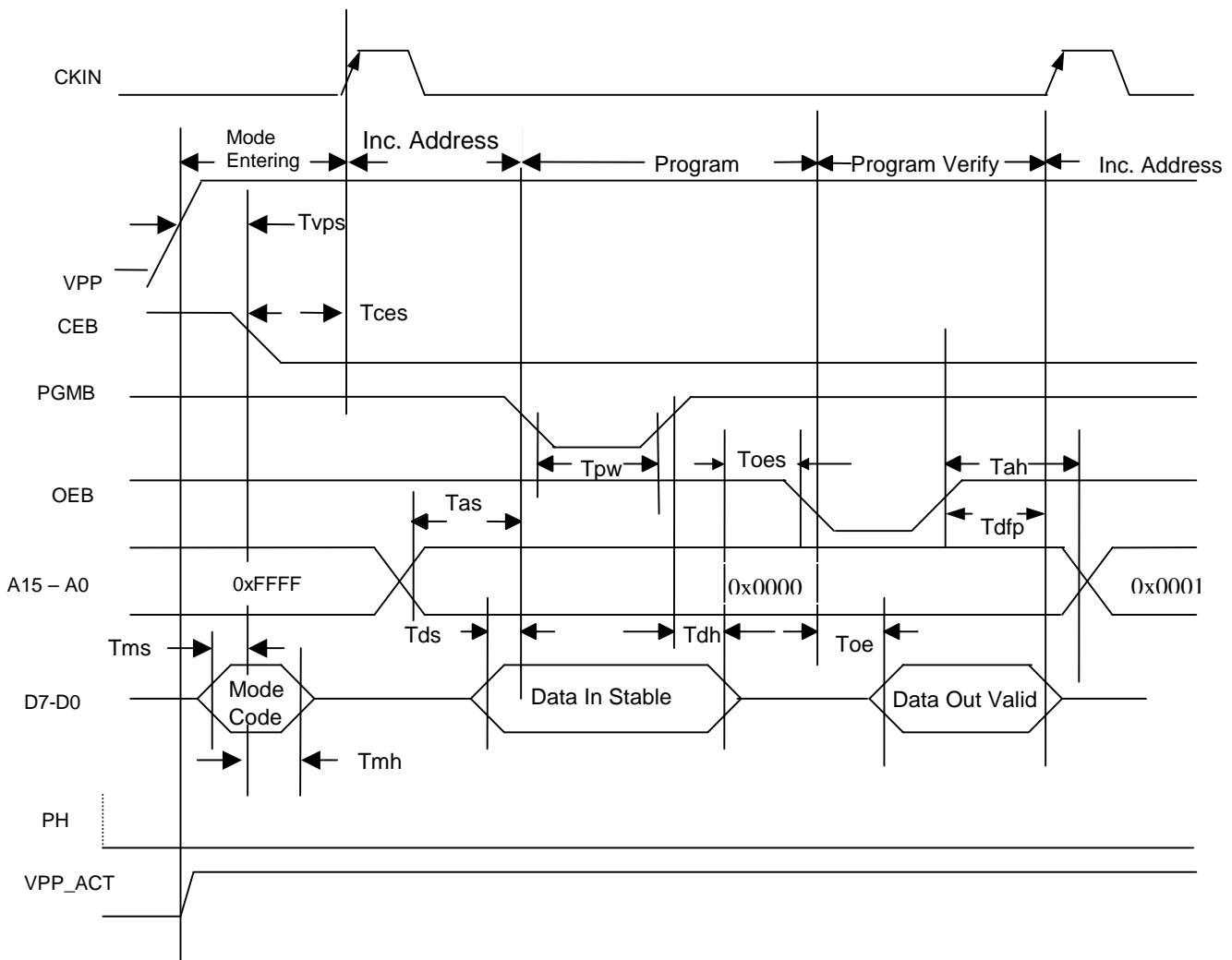
out option bits will be latched at customer's part. Customer can define all the option bit addresses as well.

**Option Bits Program & Program Verify Mode:**

It performs similarly to the normal Program & Program Verify Mode except the mode entering code is 02H. A detailed timing waveform can be referred to in Fig.3.

**OTP EPROM Program Mode Operation  
Timing AC Programming Characteristics (@Vcc=6V; Ta=25°C)**

Parameter	Symbol	OTP EPROM		Unit
		Min	Max	
Address Hold Time	Tah	0		us
Address Setup Time	Tas	2		us
OEB Setup Time	Toes	2		us
Data Setup Time	Tds	2		us
Data Hold Time	Tdh	2		us
Mode Code Setup Time	Tms	2		us
Mode Code Hold Time	Tmh	2		us
Output Enable to Output Float Delay	Tdfp	0	130	ns
VPP Setup Time	Tvps	2		us
PGMB Program Pulse Width	Tpw	95	105	us
Data Valid from OEB	Toe		100	ns
CEB Setup Time	Tces	2		us



**Fig.3 Program and Program Verify Operations Timing**

### Program & Program Verify Mode:

Program operation of OTP EPROM macro needs the procedure of entering a test mode first while 12V is applied to VPP pin, and CKIN, PH are held at 0V, OEB and PGM are held at Vcc. The program mode codes (D7-D0 = 00H) will be latched when CEB is pulling down to low. VPP\_ACT is one output signal from one high voltage detector in the VPP pad module to indicate that VPP is 12V. It can be used to reset the program counter to the final address and change the polarity of the customer's external I/O ports. Thus, the customer's external I/O ports can be used as the control pins for programming or testing purposes. Note that the customer's program counter needs to be designed as an incremental counter employed with a function to access all the addresses in the OTP EPROM macro. The external pin CKIN that is multi-functional

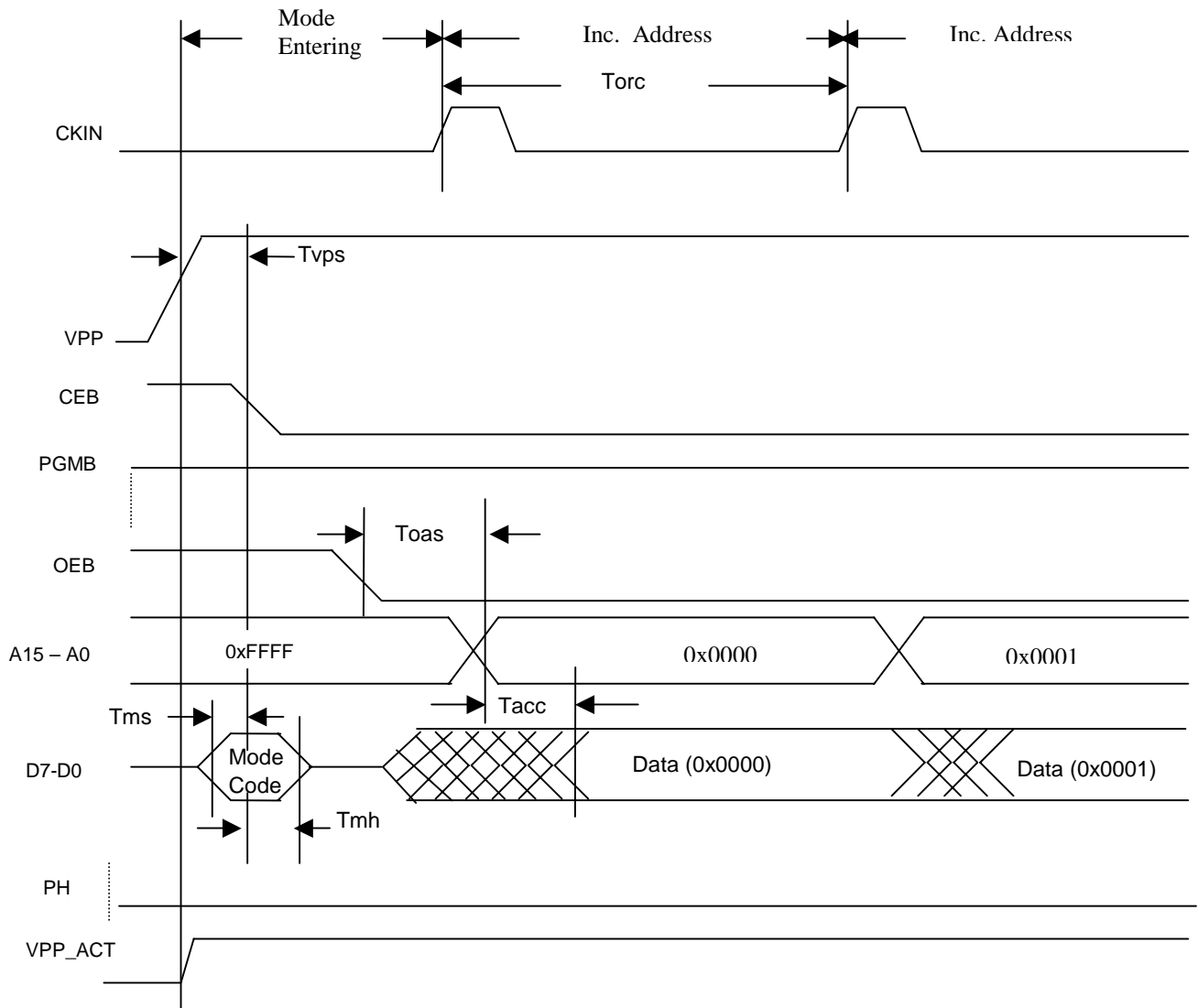
with some I/O port is used as the clock input for the program counter in the programming mode.

The write programming algorithm is achieved by applying 100us low pulse of PGMB after the address and data lines are stable and then followed by byte verification. If the data does not pass verification, additional pulse programming is applied for a maximum of 25 pulses. The programming sequence is repeated though each address by activating the associated signals such as OEB, PGMB & CKIN. The program algorithm is done at Vcc to ensure that each OTP EPROM cell is programmed to a sufficiently high threshold voltage.

As shown in the programming flow chart on page 12, the OTP EPROM macro has one byte of its bits in the “ONE”, “HIGH” or erased state to be selectively changed to “ZERO”, “LOW” or programmed state through the programming procedure.

**OTP EPROM OTP Read Mode Operation  
Timing AC Programming Characteristics (@Vcc=3.0V; Ta=25°C)**

Parameter	Symbol	OTP EPROM		Unit
		Min	Max	
OTP Read Cycle Time	Torc	80		us
Mode Code Setup Time	Tms	2		us
Mode Code Hold Time	Tmh	2		us
Address to Output Delay	Tacc		80	ns
VPP Setup Time	Tvps	2		us
OEB to Address Valid Setup Time	Toas	Torc		ns



**Fig.4 OTP Read Operations Timing**

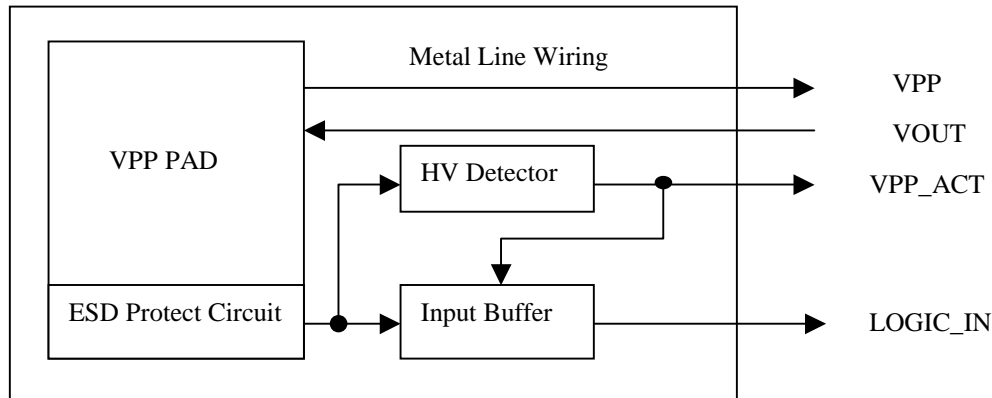
**OTP Read Mode:**

Likewise, OTP READ mode is latched while CEB is pulling down to low and D7-D0 stay at 01H during VPP = 12V. This mode is designed to test the accessing time (Tacc) from the external pins indirectly. Instead of the functional test, the read speed of the OTP EPROM macro can be verified accordingly. Owing to the same sensing design as the normal read mode, the read speed of OTP is almost the same as that of the normal read mode except for the delay between the internal data bus and output buffer. In the same manner, CKIN is used to increment the program counter and issue the

sequential address, which performs the same procedure as the previous program & program verify mode except PGMB is tied to VCC level and OEB is tied to VSS level.

### Description of VPP Pad Module

To ensure the best possible yield performance and ESD/latch-up immunity, the VPP pad module is designed by Aplus as shown in the following diagram.



**Fig.5 VPP Pad Module**

VPP PAD	VPP	VPP_ACT	LOGIC_IN
12V	12V	VCC	VCC/VSS*
VCC	VCC	VSS	VCC
VSS	VSS	VSS	VSS

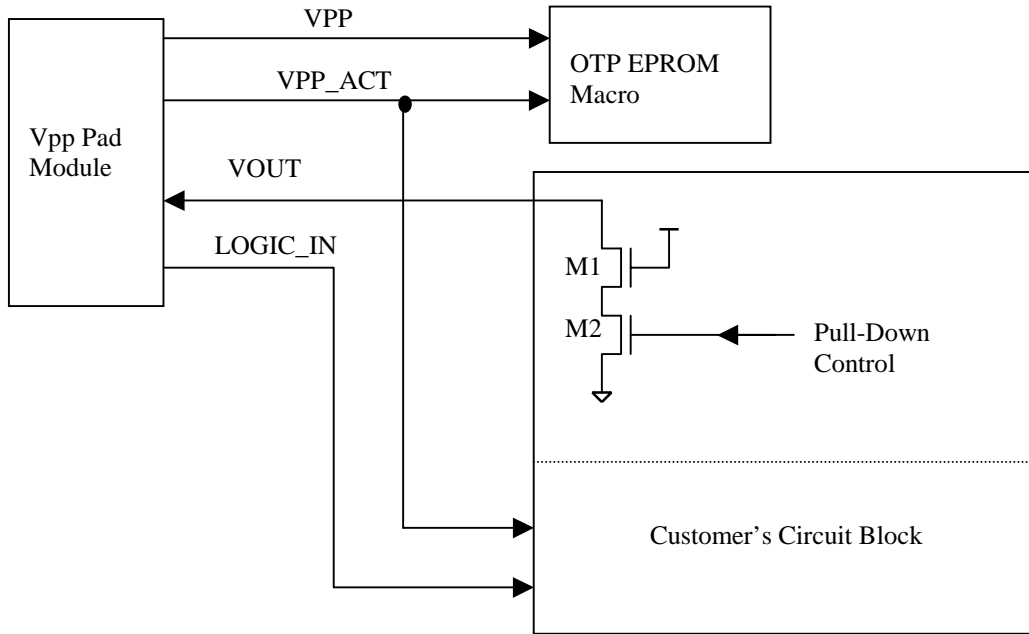
**Table. 1 Truth Table of VPP Pad**

\* : The relationship between VPP Pad & LOGIC\_IN can be determined by the customer. LOGIC\_IN will issue one logic high pulse temporarily while VPP pad is transient from 0V to 12V if the customer needs logic low at VPP = 12V. On the contrary, if the customer needs logic high at VPP =12V, there is no logic high pulse occurring as described above, instead it is held at logic high level.

As a large program current may occur during simultaneous programming of the 8 OTP EPROM cells, the metal width along the VPP line needs to be considered and made at least 10um in width. In order to avoid from any voltage drop lowering the yield, metal wiring in VPP path is required.

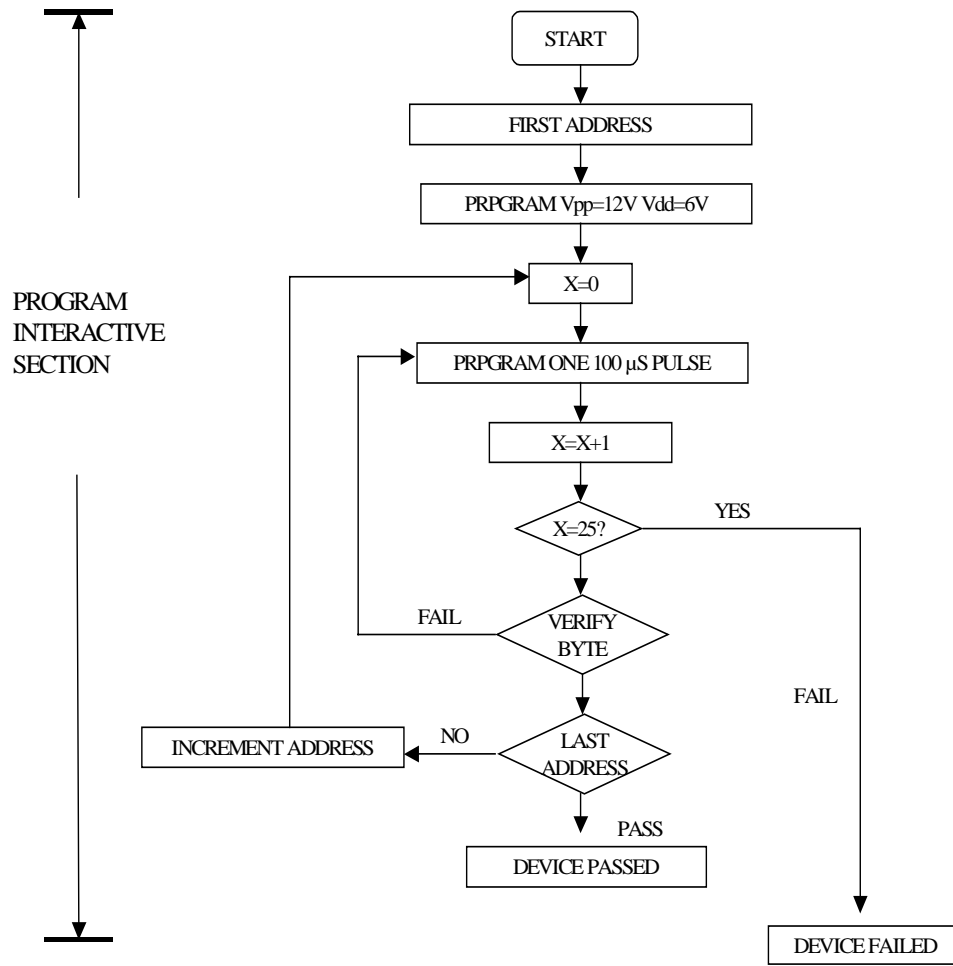
Since VPP pin will be held at 12V during programming mode, it is not allowed to connect to any source/drain side of PMOS. This is because there will be a forward current across the junction of P+/Nwell while VPP =12V is applied to source/drain and VCC is applied to N-well. However, high voltage NMOS device is allowed and is used as an output with pull down function. If the VPP pin is multiplexed with a pull down device due to the requirement of such dual function, then the customer may need to consider the design as the diagram below. The pin with pull down mechanism needs to

consist of two n-channel devices, M1 and M2, in a cascaded configuration, as shown below also. M1 will be a high voltage oxide device with a long channel length. M2 will be a low voltage oxide device with a short channel length. The width of M1 and M2 needs to be large enough to sink current in read mode. The gate of M1 will be tied to VCC. During programming (VPP = 12V) the gate of M2 will be pulled to ground.



**Fig.6 Pull-Down Output Connected to VPP Pad**

# Programming Flowchart



## REVISIONS

Version Number	Description	Page	Date
0.1	First Preliminary Draft		4/14/02

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